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MODEL 4002

TRANSMISSION AND IMPULSE NOISE DISTRIBUTION TEST SET

SERVICE MANUAL

Northeast Electronics Instruction Manual
A4002-00-601 Issue 2 September 1983

northern telecom

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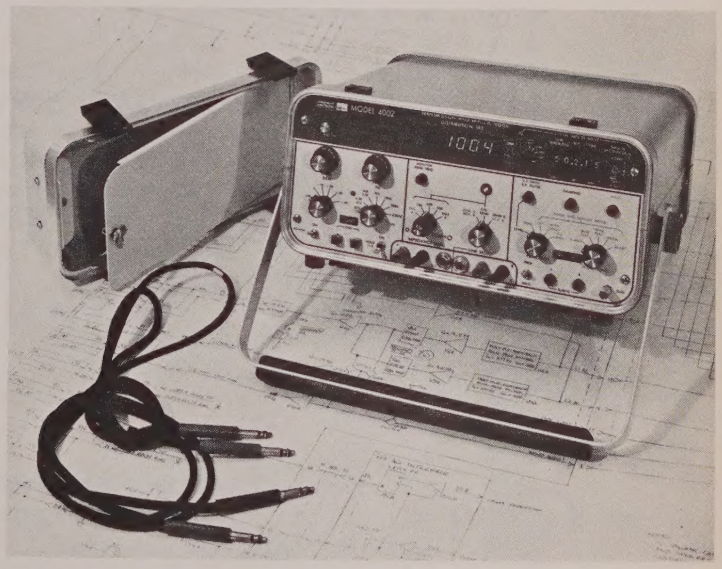

Northeast Electronics Instruction Manual
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SECTION 1

GENERAL DESCRIPTION

1.1 This manual covers the Northeast Electronics Model 4002 Transmission And Impulse Noise Distribution Set. The set is a compact, portable unit which contains a precision 3-level impulse noise counter plus all the features of a full send/receive transmission test set.

1.2 With its wideband frequency range of 35 Hz to 85 kHz, the Model 4002 is equipped to handle test requirements of nearly all telecommunications circuits in common use...including data circuits to 56 kb/s and regular voice or program circuits.

1.3 Measurements are made and displayed with digital precision on a bright, 4-digit readout. Ranging, polarity, and decimal point positioning are all fully automatic...for convenient, error-free testing.

1.4 The instrument is fully portable. It operates on 115/230 Vac or from a rechargeable battery pack which can support 5 hours of continuous use.

1.5 The 4002 is designed to the requirements of Bell Technical Reference PUB 41009.

1.6 MEASUREMENT REPERTOIRE

1.7 The 4002 is designed for fast, convenient measurement of numerous transmission parameters, including:

- ☐ Impulse noise hits...rate and distribution by amplitude..with or without holding tone
- ☐ Background noise...with or without holding tone
- ☐ Noise to ground...either background or impulse
- ☐ Signal level...and transmission loss (attenuation)
- ☐ Signal frequency...and circuit frequency shift
- ☐ Attenuation distortion (gain-slope) and circuit frequency response
- ☐ Single frequency interference
- ☐ Signal to noise ratio

Test connections can be made to either or both of two measurement channels. Either channel may be selected to receive while the other sends. And, the send/receive roles can be instantly reversed by simple switch movements.

1.8 Both channels are equipped with dial-thru and hold functions plus independently selectable impedances of 135, 600, and 900 ohms. Either terminating or bridging test connections can be selected.

1.9 These features allow easy testing of both 2-wire and 4-wire circuits. And they significantly simplify testing on a loop-around basis.

1.10 Single-switch send/receive control simplifies many common tests. When testing through loop-around equipment, the measurement direction can be instantly reversed without changing any jack connections between the 4002 and the loop.

1.11 IMPULSE NOISE MEASUREMENTS

1.12 Three adjustable thresholds and associated counting registers are incorporated in the Model 4002 to determine distributions of impulse noise hits. The base (lowest) threshold is adjustable from 10 to 99 dBrn in 1-dB steps. Separation between thresholds is selectable as 2, 4, or 6 dB...providing an overall maximum threshold of 111 dBrn (99 dBrn base threshold plus 6-dB separations for the two higher thresholds).

1.13 A precision, all-electronic timer controls the test duration. A user can select continuous measurement...or any measurement period of 0 to 99 minutes, adjustable in 1-minute steps.

The front panel digital readout is used to display:

- ☐ Total counts above low threshold
- ☐ Total counts above medium threshold
- ☐ Total counts above high threshold
- ☐ Total test time remaining (minutes)

1.14 Measurements can be made using any of the five built-in weighting filters...with or without circuit holding tone...on a balanced or noise-to-ground basis.

1.15 BACKGROUND NOISE MEASUREMENTS

1.16 Background noise measurements are displayed with 1-dB resolution. A quasi-rms detector is used. Five weighting filters are selectable:

- ☐ C-message
- ☐ 3-kHz flat
- ☐ 15-kHz flat
- ☐ Program
- ☐ 50-kb/s data

1.17 Metallic (balanced) noise measurements can be made with or without a holding tone on the circuit. A 1010-Hz notch filter meeting Bell specifications is switched in when noise-with-tone measurements are selected. Holding tone presence is easily monitored via a built-in speaker.

1.18 Noise to ground (common mode) measurements can also be made, and the results are read directly as true values between 50 and 135 dBrn. There is no need to add 40 dB as with many other test sets.

1.19 These features make the 4002 useful for noise problem diagnosis as well as routine maintenance testing. The direct reading noise to ground measurements help to identify and locate noise problems caused by:

a. power influence,

b. unbalance in the telephone office or outside plant, and

c. various types of cable faults.

1.20 For all background noise measurements, the 4002 uses a sampling rate which presents the excursions of varying noise levels with the same "feel" as on an analog meter. A long term average value for measured noise can also be viewed by switching in the 4002's noise averaging feature.

1.21 Another special feature helps identify sources of single frequency interference. This feature counts and displays the frequency of any signal which is predominant in the filter-weighted input noise spectrum. Discrimination is built into the test set so that only the major interfering signal is counted; spurious energy at lower amplitude is ignored.

1.22 This feature helps to quickly detect such noise problems as:

- ☐ 60 Hz and its harmonics
- ☐ Leaky SF
- ☐ Spurious network tones

1.23 LEVEL MEASUREMENTS

1.24 Signal level measurements are displayed directly in dBm. Resolution is 0.1 dB over the entire −70 to +15 dBm measurement range. Full wave averaging is the detection method. A 200 Hz to 10 kHz bandpass filter may be switched in if needed to suppress low and/or high frequency noise present on a circuit under test.

1.25 FREQUENCY MEASUREMENTS

1.26 The 4002 counts and displays frequencies in the range from 20 Hz to 85 kHz. Frequencies up to 9999 Hz are displayed with resolution of 1 Hz. Above 9999 Hz, the measurements are displayed in kHz units, with resolution of 10 Hz. The decimal point is always positioned automatically, via autoranging.

1.27 The 4002's frequency counting capabilities are ideal for checking frequency shift introduced by a communications circuit, a measurement most important when carrier facilities are involved. The 4002's combination of frequency and level measurement capabilities make it well suited for setting up and periodically checking the output of SF, MF, and other ac signaling tone sources.

1.28 SEND SECTION

1.29 A dual coarse/fine tuning control allows the transmitter to be rapidly, yet precisely set at any frequency in a 35 Hz to 60 kHz range. In addition, individual frequencies of 404, 1004, 2804 Hz...plus 82 kHz...are switch selectable. The three lower frequencies are convenient for attenuation distortion (gain-slope) measurements, and the 1004 Hz position is also helpful whenever a regular milliwatt or holding tone is required. The 82 kHz position is useful when testing DDS private line local loops per BSP 14-410-510.

1.30 Transmitted signals can be very accurately set at any level from +13 to −50 dBm. The transmitter output is extremely stable in both frequency and amplitude.

SECTION 2

SPECIFICATIONS

2.1 The major specifications of the Model 4002 test set are listed in Table 2–1. Frequency response information for the bandpass and noise weighting filters is shown in Figures 2–1 through 2–6.

Table 2–1. Overall Specifications

RECEIVE SECTION

BACKGROUND NOISE MEASUREMENTS

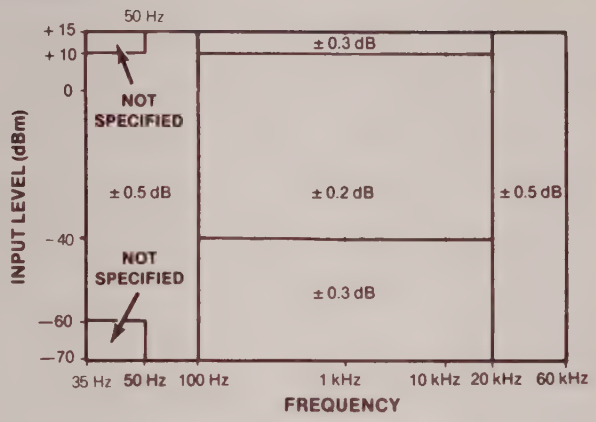
Circuit Noise Range:	0 to 85 dBrn for 600 or 900 ohms 10 to 85 dBrn for 135 ohms
Noise With Tone Range:	10 to 85 dBrn for 600 or 900 ohms 20 to 85 dBrn for 135 ohms
Noise To Ground Range:	50 to 135 dBrn
Resolution:	1 dB
Sampling Rate:	2.5 per second
Detection Method:	full-wave quasi-rms
Circuit Noise Accuracy:	±1 dB from 0 to 85 dBrn for 600 or 900 ohms ± 1 dB from 10 to 85 dBrn for 135 ohms
Noise With Tone Accuracy: (holds over full 0 to 50°C temperature range)	±1 dB from 10 to 85 dBrn for 600 or 900 ohms ±1 dB from 20 to 85 dBrn for 135 ohms
Noise To Ground Accuracy: (holds over full 0 to 50°C temperature range).	±1.5 dB from 50 to 135 dBrn scaled for 600 or 900 ohm circuits ±1.5 dB from 60 to 135 dBrn scaled for 135 ohm circuits
Weighting Filters:	C-message (see Figure 2–1) 3-kHz flat (see Figure 2–2) 15-kHz flat (see Figure 2–3) Program (see Figure 2–4) 50-kb/s (see Figure 2–5) Optional CCITT filter can be substituted for C-message filter.
Notch Filter:	centered at 1010 Hz
Noise Variation Averaging: (damping)	selectable feature displays long-term average noise value on digital readout
Single Frequency Interference:	selectable feature displays frequency of any predominant signal (15 dB peak S/N ratio) in filter weighted input noise spectrum

Table 2—1. (Cont'd).

IMPULSE NOISE DISTRIBUTION MEASUREMENTS	
Threshold Range:	
☐ Balanced	10 to 111 dBrn into 600, 900 ohms with C-message filter
	20 to 111 dBrn into 600, 900 ohms with all filters
	30 to 111 dBrn in 135 ohms with all filters
☐ Noise To Ground	60 to 140 dBrn in 600 ohms with C-message filter
Threshold:	
☐ Lowest	selectable from 10 to 99 dBrn in 1-dB steps
☐ Number	3
☐ Separation	selectable 2, 4, or 6 dB
☐ Accuracy	±1 dB
Turnover:	0.2 dB
Timing:	selectable from 1 to 99 minutes in 1-minute steps.
Timing Accuracy:	±1 second of setting
Counting Rate:	7 pps (143±7 msec)
Blanking Interval:	per Bell Technical Reference PUB 41009
Detector Response:	per Bell Technical Reference PUB 41009
LEVEL MEASUREMENTS	
Frequency Range:	35 Hz to 85 kHz
Level Range:	−70 to +15 dBm
Resolution:	0.1 dB
Sampling Rate:	6 per second
Detection Method:	full-wave averaging
Absolute Accuracy At 1 kHz: (holds over 0 to 50°C temperature range with 135, 600, 900 ohms impedance)	±0.3 dB from +10 to +15 dBm ±0.2 dB from −40 to +10 dBm ±0.3 dB from −70 to −40 dBm

Table 2—1. (Cont'd).

Frequency Response:



Note: For measurements at 135 ohms, accuracy between 100 and 250 Hz is ±0.5 dB; accuracy is not specified below 100 Hz.

Accuracy Versus Temperature: (holds over 0 to 95% relative humidity range)	±0.0025 dB/°C at 1 kHz
Bandpass Filter: (noise protection)	200 Hz to 10 kHz bandpass (refer to Figure 2—6)

FREQUENCY MEASUREMENTS

Range:	20 Hz to 85 kHz
Resolution:	
20 Hz to 9999 Hz	1 Hz
10 kHz to 85 kHz	10 Hz
Sampling Rate:	4 per second
Accuracy:	±1 count (LSD)

SEND SECTION

Variable Frequency Range:	35 Hz to 60 kHz continuously variable in 3 ranges; can be set to ±1 count accuracy using the digital readout
Fixed Frequencies:	selectable 404, 1004, 2804 Hz, and 82 kHz
Fixed Frequency Stability: (404, 1004, 2804 Hz)	±0.1% per hour after an initial warm-up of one minute
Output Level Range:	−50 to +10 dBm into 135, 600, and 900 ohms −50 to +13 dBm into 135 and 600 ohms at 200 Hz to 4 kHz Minimum +7.5 dBm into 135 ohms at 82 kHz Vernier fine adjust range 13 dB min to 15 dB max
Output Level Accuracy:	Can be set to accuracy limits of receive section without accessory instruments
Flatness for 600 or 900 Ohms:	±0.5 dB from 35 Hz to 200 Hz ±0.2 dB from 200 Hz to 15 kHz ±0.5 dB from 15 kHz to 50 kHz ±1.5 dB from 50 kHz to 60 kHz

Table 2—1. (Cont'd).

Flatness For 135 Ohms:	±0.5 dB from 60 Hz to 200 Hz ±0.2 dB from 200 Hz to 15 kHz ±0.5 dB from 15 kHz to 50 kHz ±1.5 dB from 50 kHz to 60 kHz
Output Level Stability:	±0.05 dB per hour after an initial warm-up of one minute
Distortion: (holds at any output level for any output impedance)	≤40 dB from 40 Hz to 100 Hz ≤50 dB from 100 Hz to 3.5 kHz ≤40 dB from 3.5 kHz to 60 kHz
Crosstalk:	per Bell Technical Reference PUB 41009

GENERAL

Input/Output Balanced Impedances:	135, 600, or 900 ohms
Input Return Loss: (without holding circuit)	≥30 dB from 500 Hz to 50 kHz for 135 ohms ≥30 dB from 100 Hz to 20 kHz for 600 or 900 ohms
Output Return Loss: (without holding circuit)	≥30 dB from 500 Hz to 20 kHz for 135 ohms ≥30 dB from 100 Hz to 20 kHz for 600 or 900 ohms
Input/Output Return Loss: (with holding circuit)	same as without hold circuit except that below 300 Hz and above 10 kHz, the return loss specification is relaxed by 6 dB/octave when in 600 or 900 ohms. Not specified for 135-ohm circuits.
Input/Output Longitudinal Balance:	≥80 dB at 60 Hz ≥60 dB for frequencies ≤ 4 kHz; decreases by 6 dB/octave above 4 kHz
Input Bridging Impedance: (without holding circuit)	≥25 kohms at 1 kHz for 135, 600, or 900 ohms
Input Bridging Loss: (with holding circuit)	≤0.2 dB from 100 Hz to 60 kHz for 135 ohms ≤0.2 dB from 100 Hz to 20 kHz for 600 ohms ≤0.3 dB from 100 Hz to 60 kHz for 900 ohms
Input Noise To Ground Impedance:	100 kohms tip to ring; 100 kohms tip to ground or ring to ground
Input Common Mode Rejection:	per Bell Technical Reference PUB 41009
Line Holding:	passive hold coil with 470 ohms dc resistance
Input/Output Protection:	300 Vdc blocking, both bridging and terminating 200 Vdc noise-to-ground
Power:	115 or 230 Vac, 48 to 440 Hz Optional rechargeable battery pack supplies up to 5 hours of continuous operation
Temperature Range:	operating: 0°C to 50°C (32°F to 122°F) storage: −20°C to 65°C (−4°F to 149°F)
Relative Humidity:	0 to 95% at ≤40°C (≤104°F) 0 to 85% at ≤50°C (≤122°F)

Table 2—1. (Cont'd).

Size: (wxhxd)	
4002 unit	16-3/4 × 6-3/8 × 11-3/4 (43 × 16.2 × 29.8 cm)
Battery Pack	11-1/2 × 5-1/2 × 1-5/8 in. (29.2 × 14 × 4.2 cm)
Weight:	
4002 unit	24 lb. (10.9 kg)
Battery Pack	6-¾ lb. (3.1 kg)

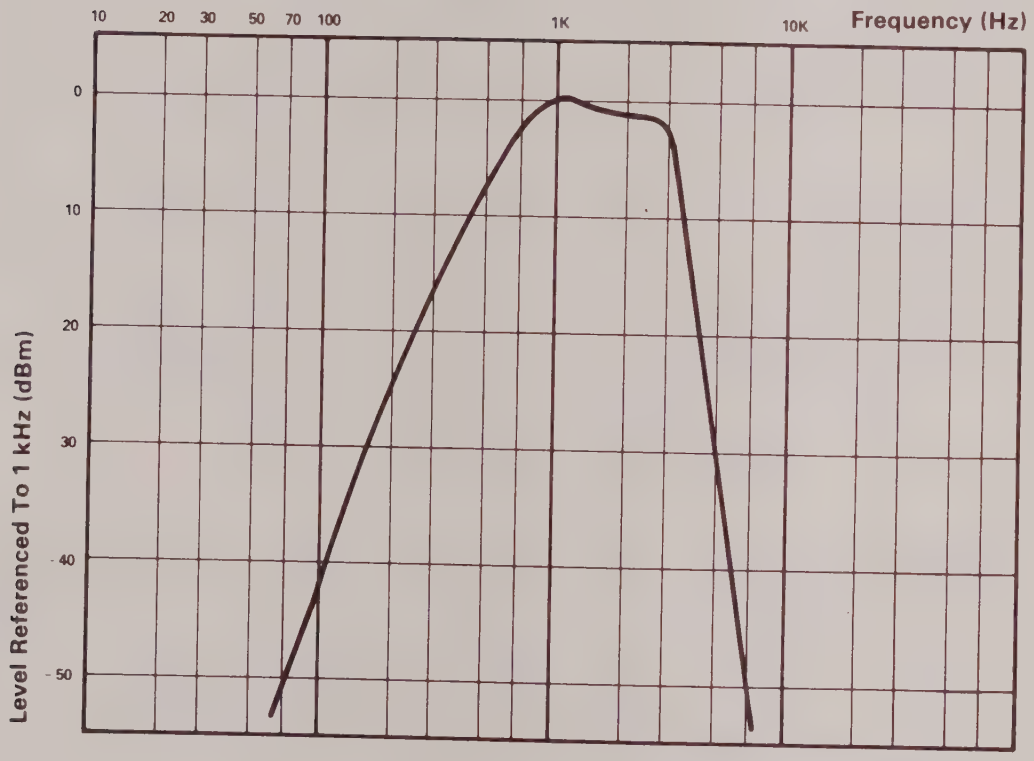


Figure 2—1. C-Message Filter Frequency Response.

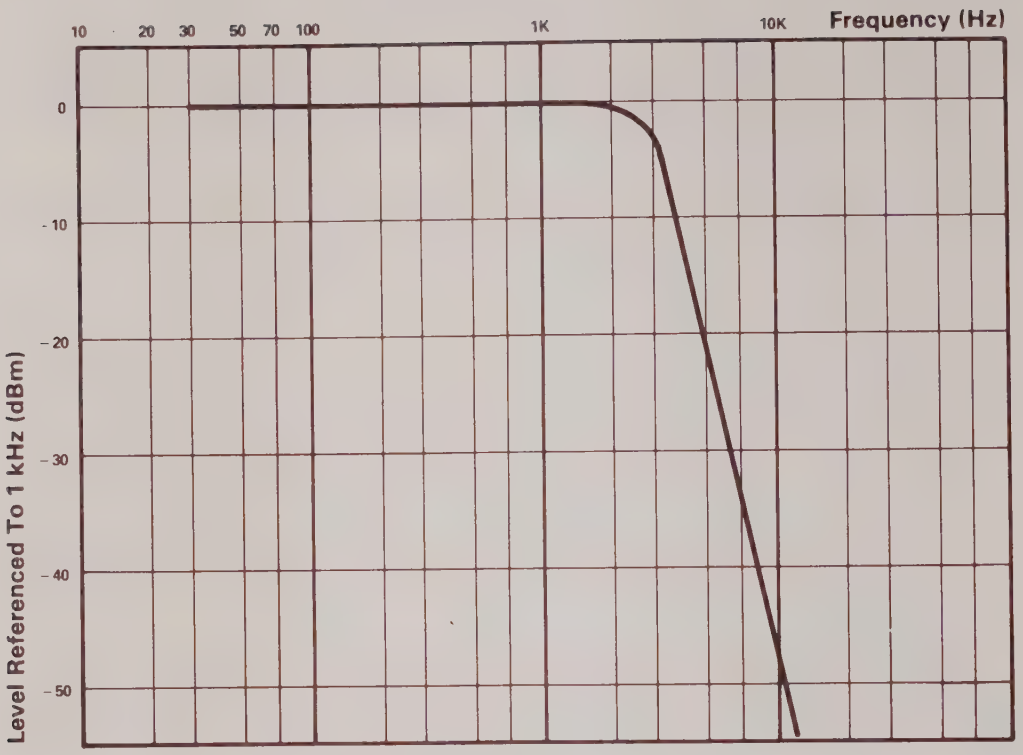


Figure 2—2. 3-kHz Flat Filter Frequency Response.

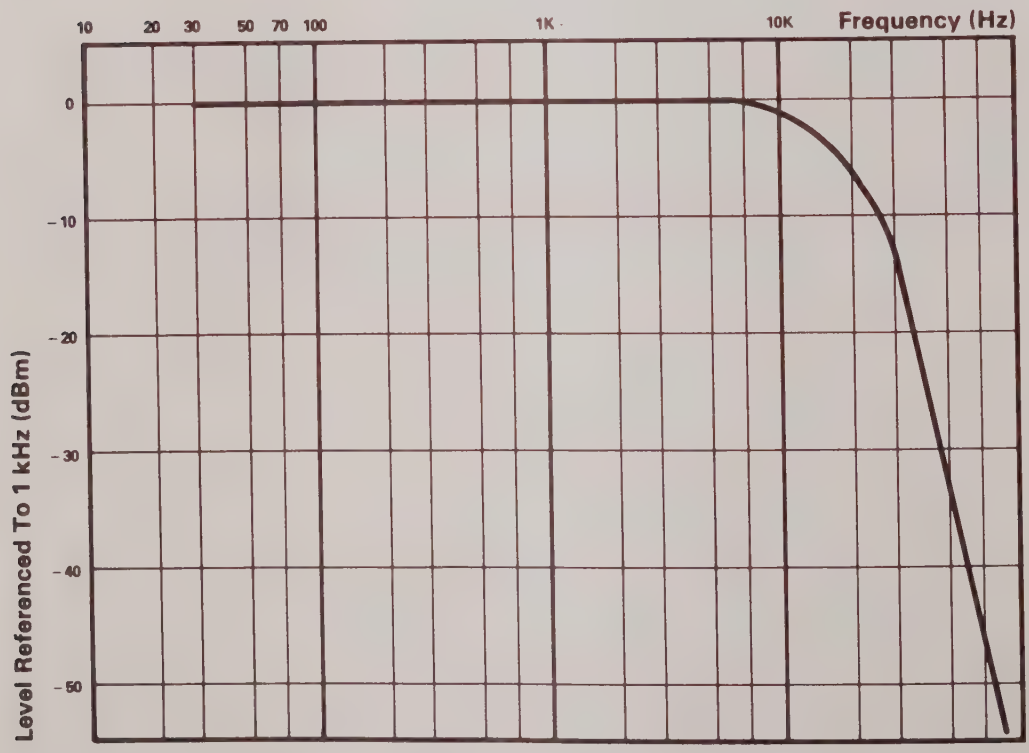


Figure 2—3. 15-kHz Flat Filter Frequency Response.

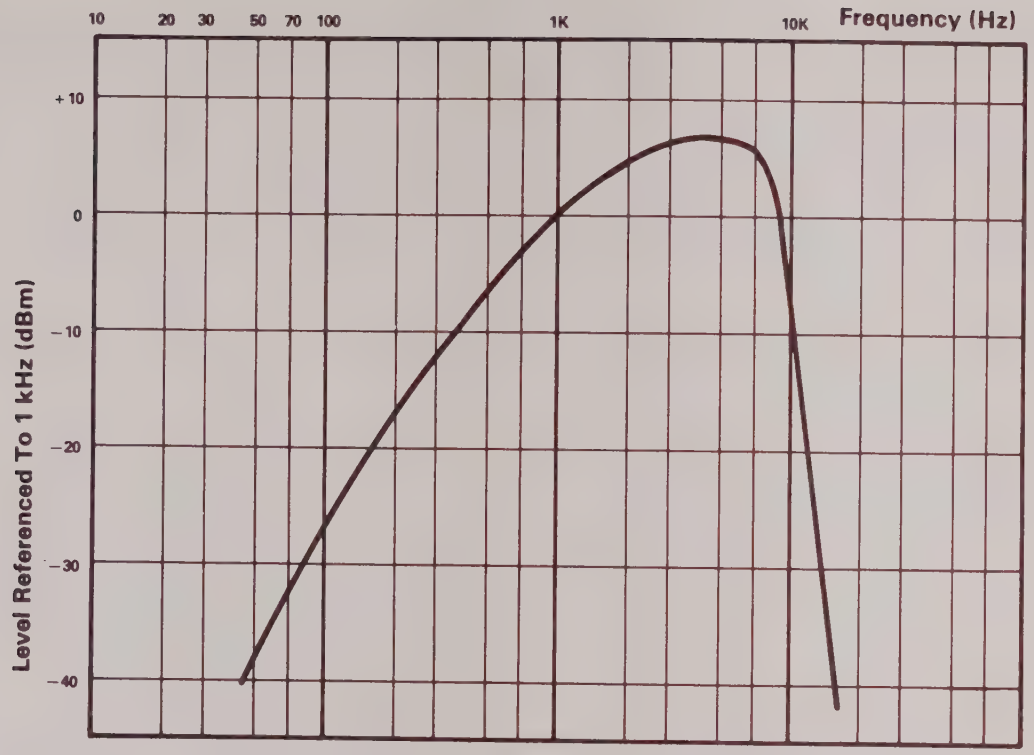


Figure 2—4. Program Filter Frequency Response.

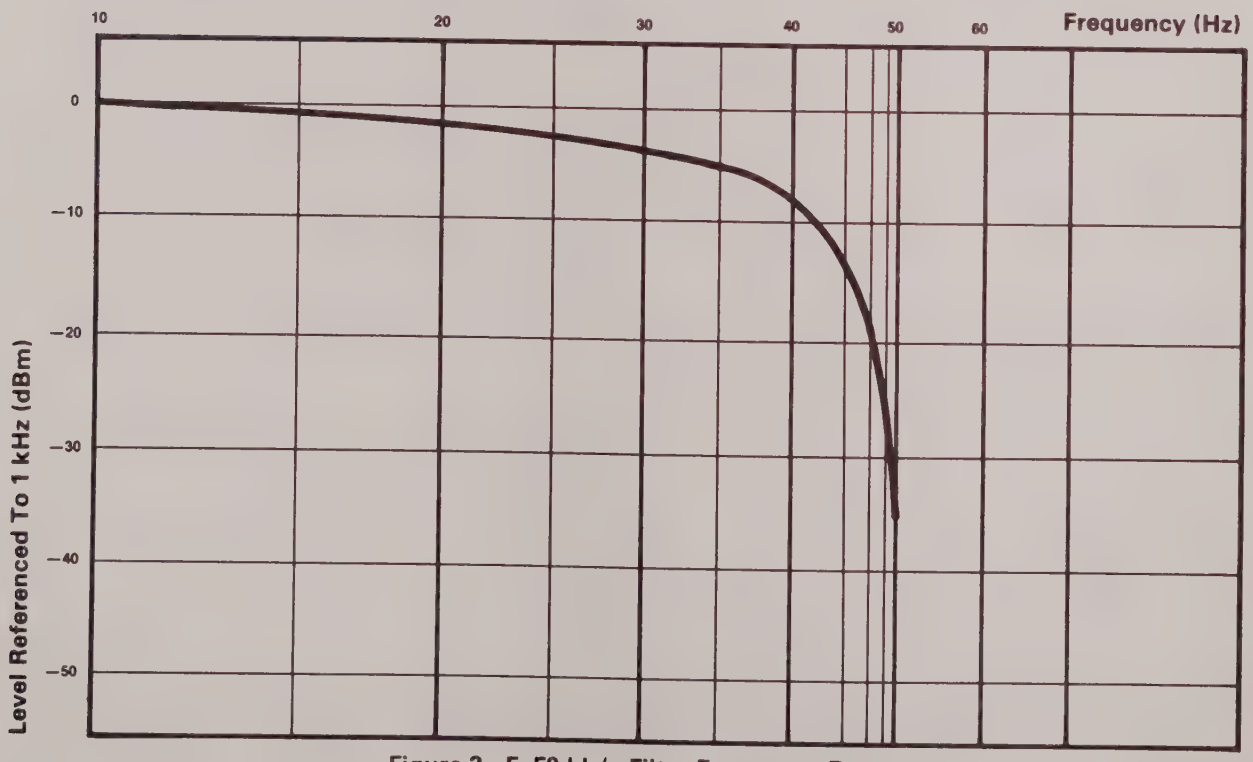


Figure 2—5. 50-kb/s Filter Frequency Response.

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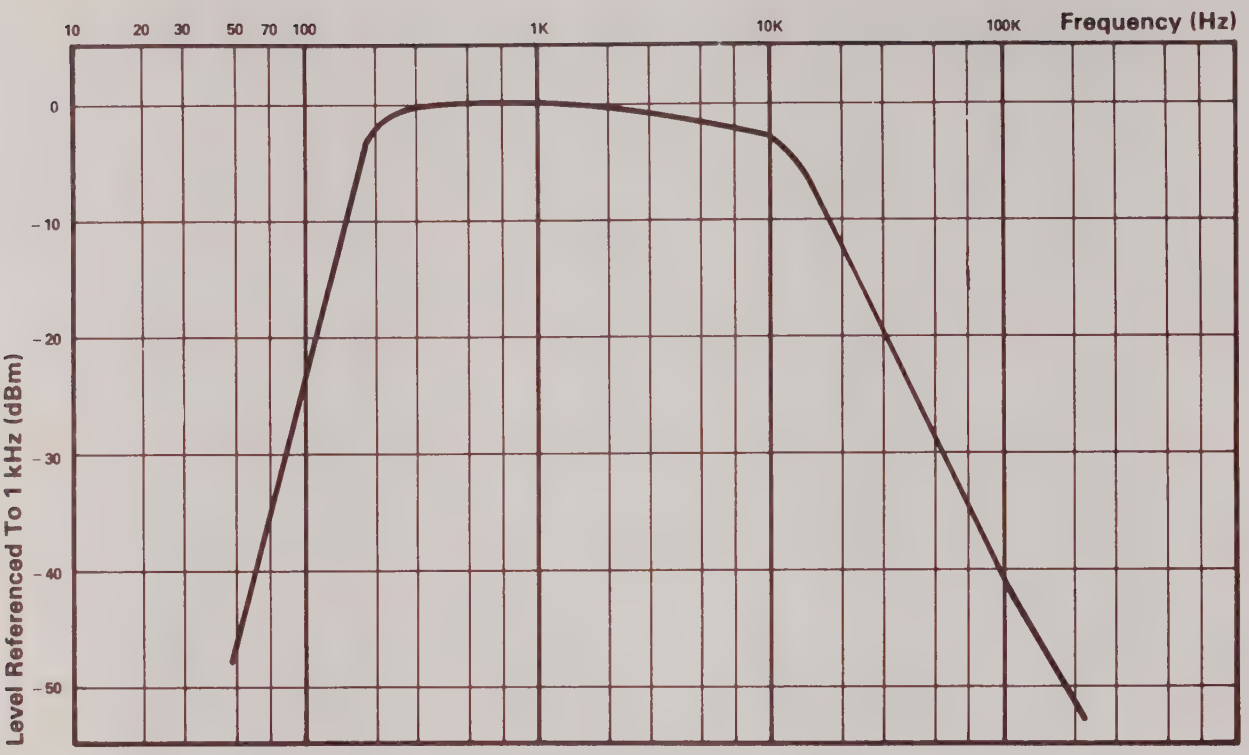


Figure 2—6. Bandpass Filter Frequency Response.

SECTION 3

TEST SET PREPARATION

3.1 This section contains information needed for preparing the Model 4002 Transmission And Impulse Noise Distribution Set for test. The information includes:

1. Service information
2. Interface requirements
3. Preparation for use
4. Battery pack installation

3.2 SERVICE INFORMATION

3.3 Complete warranty information is contained in the purchase order agreement under terms and conditions of sale. Summarized briefly, the Northeast Electronics warranty extends for a period of one year to the original purchaser of a Northeast Electronics product.

3.4 It is recommended that Northeast's Repair Department be contacted for assistance if, for any reason, a Northeast product fails to perform as expected. This step eliminates the needless delay entailed when a product is returned to the factory unnecessarily. Contact the Repair Department at Northeast Electronics, P.O. Box 649, Concord, New Hampshire 03301, telephone: (603) 224-6511.

3.5 If a Northeast Electronics product requires factory servicing **during** the warranty period, be sure to include a ship-to address and a description of the problem when returning the product to Northeast Electronics. **After** the warranty period has expired, equipment returned must be accompanied by all of the following:

- ☐ The number of the purchase order covering the cost of servicing,
- ☐ Bill-to address,
- ☐ Ship-to address,
- ☐ Description of problem.

3.6 In all cases, equipment requiring factory servicing should be sent to the Repair Department at the preceeding address and telephone number. A return material authorization (RMA) number is **not** required, but will be provided by the Repair Department upon request.

3.7 INTERFACE REQUIREMENTS

3.8 The set is equipped with two types of input/output connectors. The T and R connectors are standard size binding posts. These binding posts are spaced to accept a standard dual banana plug. The other type of connector is for the WECO 310 plug. Northeast Electronics specially designed the DIAL connector post for quick and convenient attachment of a lineman's handset.

3.9 TEST SET PREPARATION FOR USE

3.10 The set requires very little preparation for use. Place the test set on a convenient work surface and remove the front cover. Secure the carrying handle in a position to tilt the test set at a convenient viewing angle.

3.11 BATTERY PACK INSTALLATION

3.12 The Model 4002 can be operated from an external ac power source or an optional battery pack. To mount the battery pack:

1. Orient the battery pack to face the rear of the test set with the large batteries (12V batteries) at the bottom of the pack.
2. Connect the battery cable to battery jack J15.
3. Secure the battery pack to the test set with the slide catches.

SECTION 4

OPERATION

4.1 This section provides the information needed for operation of the Model 4002 Transmission And Impulse Noise Distribution Set. The information is organized as follows:

a. AC power operation

b. Battery pack operation

c. Grounding requirements

d. Brief descriptions of test set measurement capabilities

e. Description of all connectors, switches, controls, and indicators.

4.2 AC POWER OPERATION

4.3 The set can be operated from any power source supplying 105 Vac to 129 Vac or 210 Vac to 258 Vac, 48 Hz to 440 Hz. Check the setting of the 115/230 switch located at the rear of the set before applying power. Power dissipation is 20 VA maximum.

CAUTION

If the instrument is not set for the power primary voltage and not properly fused, it may be seriously damaged.

4.4 If it is necessary to change the primary voltage, perform the following steps.

1. Ensure that the test set is disconnected from the external power source and the POWER switch is off.

2. Slide the 115/230 switch at the rear of the test set to the desired primary ac voltage.

3. Check to ensure that you are using the proper fuse. A 0.3 amp slo-blow fuse is required for 115 Vac line operation. A 0.2 amp slo-blow fuse should be used for 230 Vac line operation.

4.5 BATTERY PACK OPERATION

4.6 The optional battery pack consists of three rechargeable batteries (+6V, +12V, and −12V) which provide up to 5 hours of continuous use. Refer to Section 3 for battery pack installation. The set has a sensing circuit which monitors the three battery voltages. If any battery voltage falls below the minimum operating level (−4.8V for the +6V battery and 10.8V for the 12V batteries), the voltages to all circuits in the set are automatically switched off to prevent any possibility of erroneous measurement data readouts.

NOTE

If the digital display ever goes completely blank (when operating on the battery pack) with POWER switch set at ON, then the sensing circuit has probably switched the set off.

4.7 The battery pack should be charged whenever possible. To recharge the battery pack:

1. Remove the battery pack from the test set without disconnecting the battery pack cable.

2. Verify that the fuses are of the proper rating and have not blown. (Refer to paragraph 4.4.)

3. Connect the test set to an ac power source. Recharging time is 12 to 22 hours.

NOTE

The test set may be used while charging a battery pack.

4.8 Batteries charged frequently have a longer lifetime and provide maximum operating time. The battery pack performance improves when operated under cyclical conditions (alternate charge and discharge). In fact, the normal battery capacities may not be reached until 50 or more charge/discharge cycles are completed. A fresh battery pack may not provide 5 hours of service initially.

CAUTION

If, after normal recharging period (12 to 22 hours), the test set operates in battery mode for less than 3 hours, then one of the batteries is not holding a charge or a charging circuit is defective. Remove and disconnect the battery pack. Operate the test set on ac power source.

CAUTION

The batteries must not remain in a discharged or partially discharged condition for more than two days. Chemical reaction within the batteries may reduce battery capacity and lifetime. A totally discharged battery stored for an extended period can later fail to accept a charge.

4.9 Batteries **must** be charged for at least 48 hours before extended storage (two weeks or more) regardless of battery charge condition. Preferred storage temperature is 21°C (70°F) or below. Storage at temperatures above 38°C (100°F) should be avoided. Stored batteries must be recharged at least twice per year. Higher temperatures require more frequent charging. This boost charge insures maximum battery life and performance.

4.10 GROUNDING REQUIREMENTS

4.11 To protect operating personnel, the National Electrical Manufacturer's Association (NEMA) recommends that the instrument panel and cabinet be grounded. The set is equipped with a three-conductor power cable which, when plugged into an appropriate receptacle, grounds the set.

WARNING

To ensure operator protection, connect the front panel ground terminal to earth ground when operating on the battery pack.

4.12 TEST SET CAPABILITIES

4.13 The set can measure circuit noise, impulse noise distribution, level and frequency of tones on telecommunication circuits while simultaneously providing calibrated test signals. The Model 4002 can test data, program, and voice circuits. The set accepts both two-wire and four-wire balanced circuits. Frequency and level measurement can be made either in a bridged or terminated mode. The send and receive impedances can be individually set at 135, 600, or 900 ohms.

4.14 Additional features of the set include:

1. Digital LED display of measurement results;

2. Autoranging in most modes;

3. Fixed time constants and sampling rate for tone, frequency, and noise measurements;

4. Dial and hold facilities for each input/output channel;

5. A choice of five weighting noise filters (C-message, 3-kHz flat, 15-kHz flat, program, or 50-kb/s).

4.15 CONTROLS AND INDICATORS

4.16 Figure 4—1 shows the front panel and Figure 4—2 shows the rear panel. Table 4—1 briefly describes the functions of each control, indicator, or jack. The controls, indicators, and connectors have been arranged into functional groups in Table 4—1. The functional groups are : (1) monitor/display, (2) impulse noise, (3) send, (4) impedance/line select, (5) receive, (6) dial/hold, (7) power, and (8) rear panel.

4.17 BASIC OPERATING PROCEDURES

4.18 Paragraphs 4.20 through 4.26 give step procedures for:

a. Dial and hold operation;

b. Making background noise and impulse noise measurements;

c. Making level and frequency measurements;

d. Send section operation.

4.19 The set should be allowed to warm-up for one minute before use. This allows the send section to stabilize.

4.20 DIAL AND HOLD PROCEDURE

NOTE

Procedure written for Line A. Instructions for Line B are in parenthesis.

1. Set HOLD A + B switch at ON, if required.

2. Connect a lineman's handset to the square dial posts.

3. Connect a circuit to the 310 jack or to the T and R binding posts of the A (or B) input/output line.

4. Set LINE select switch at SEND B/RCV A (or SEND A/RCV B).

5. Set RECEIVE IMPEDANCE switch at 135, 600, 900 as required.

6. Set SEND IMPEDANCE (DIAL) switch at DIAL A (or DIAL B).

7. Place the lineman's handset off-hook.

8. Dial with the lineman's handset.

9. When the dialed connection is completed, set the SEND IMPEDANCE at 135, 600 or 900 (any impedance suffices).

10. Place the lineman's handset on-hook.

4.21 CIRCUIT NOISE AND NOISE WITH TONE MEASUREMENT PROCEDURE

1. Connect circuit under test to the 310 jack or to the T and R binding posts of the desired input (line A or B).

2. Set LINE SELECT switch at SEND A/RCV B or at SEND B/RCV A, depending on the input connections made is step 1.

3. Set both RECEIVE and SEND IMPEDANCE (DIAL) switches at the circuit-under-test impedance(s).

4. Set IMPULSE COUNTER switch at OFF/RESET.

5. Set line TERM/BRDG switch as desired.

6. Set FUNCTION switch at CKT or at WITH TONE.

NOTE

Holding tone normally transmitted at −13 to −16 dBm.

7. Set WEIGHTING switch for the desired noise filter.

8. Read noise level in dBrn directly on the digital display.

9. If desired, press DAMPING switch to see long term noise value on display.

10. If desired, press FREQ switch to obtain indication of single frequency interference. The digital display will show a stable frequency count in the presence of a single tone having a signal-to-noise ratio greater than 15 dB.

NOTE

Presence of tone can be heard on monitor speaker.

NOTE

A blank display with a plus sign indicates the input noise level is above 85 dBrn. A blank display with a minus sign Indicates the input noise level is below 0 dBrn.

4.22 NOISE TO GROUND MEASUREMENT PROCEDURE

1. Connect the circuit under test to the 310 jack or to the T and R binding posts of the desired input (line A or B).

2. Set LINE SELECT switch at SEND A/RCV B or at SEND B/RCV A, depending on the connections made in step 1.

3. Set the RECEIVE and SEND IMPEDANCE (DIAL) switches to 600.

NOTE

Normally, noise to ground measurement calibration requirements reflect the equivalent measured voltage in a 600-ohm impedance. However, the Model 4002 can be set to measure noise to ground corresponding in calibration equivalent to 135-ohm or 900-ohm impedances, if desired.

4. Set IMPULSE COUNTER switch at OFF/RESET.

5. Set FUNCTION switch at TO GND.

6. Set WEIGHTING switch for the desired noise filter.

7. Read noise level in dBrn directly on digital display. **No correction is required.**

8. If desired, press DAMPING switch to see long term noise value on display.

9. If desired, press FREQ switch to obtain indication of single frequency interference. The digital display will show a stable frequency count in the presence of a single tone having a signal-to-noise ratio greater than 15 dB.

NOTE

Presence of tone can be heard on monitor speaker.

NOTE

A blank display with a plus sign indicates the input noise level is above 135 dBrn. A blank display with a minus sign indicates the input noise level is below 50 dBrn.

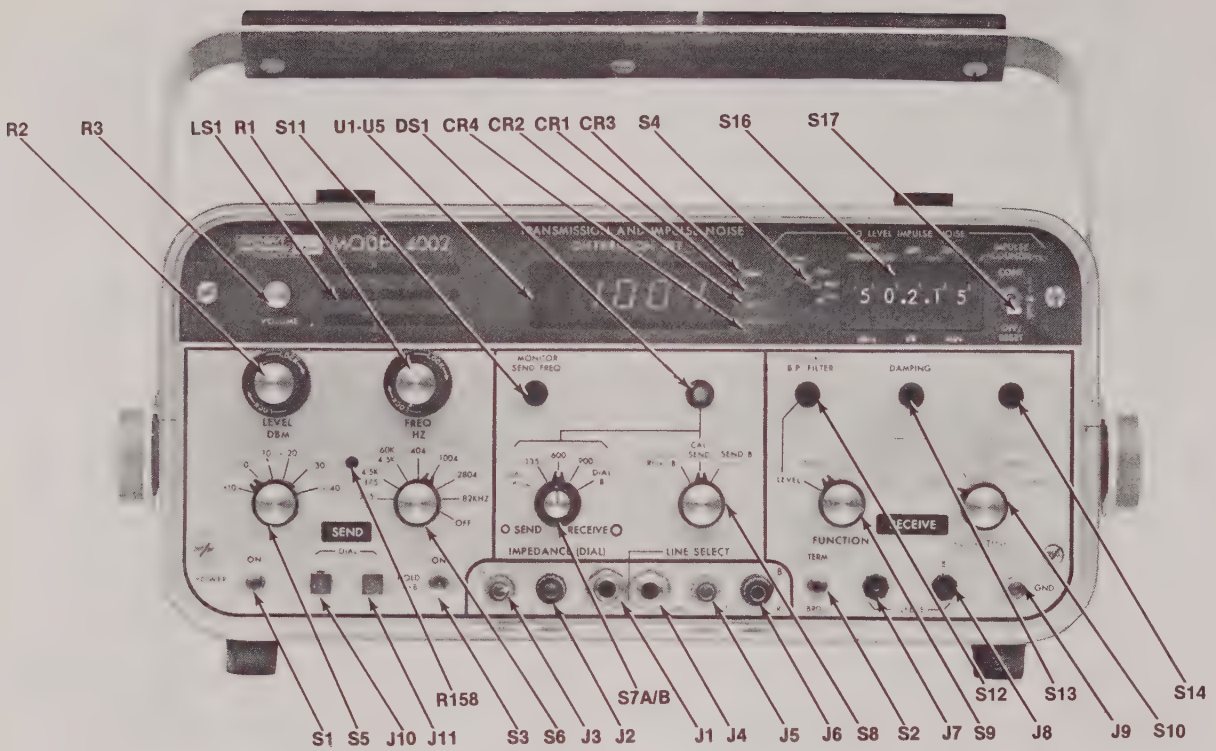


Figure 4—1. Front Panel Controls.

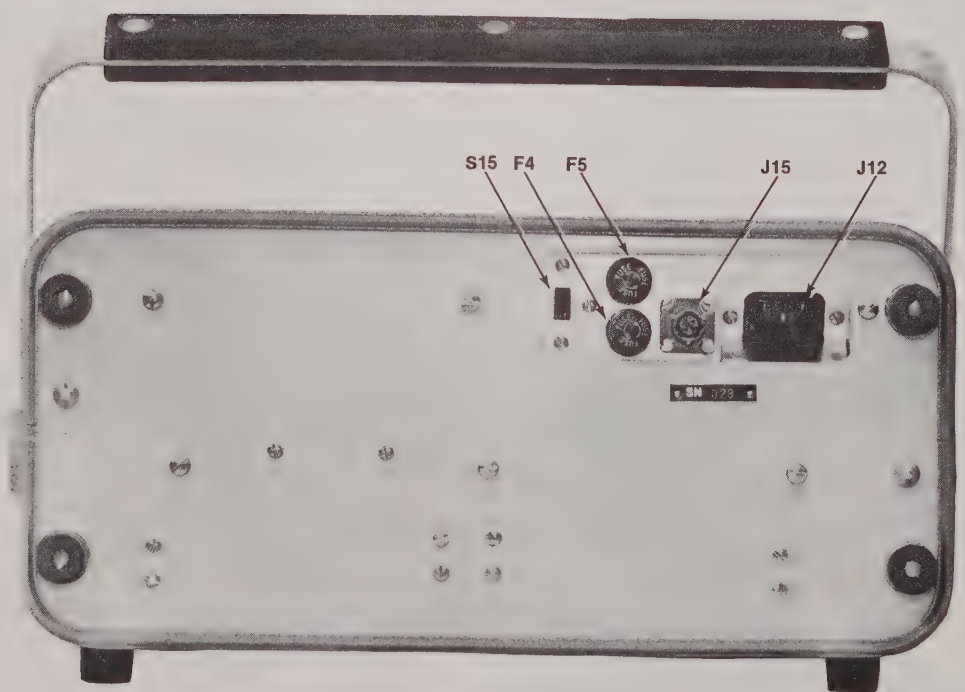


Figure 4—2. Rear Panel Controls.

Table 4—1. Controls, Indicators, And Jacks

REFERENCE DESIGNATION	NOMENCLATURE	DESCRIPTION
MONITOR AND DISPLAY		
R3	VOLUME potentiometer	Adjusts the sound level heard on the audio monitor speaker. A portion of the receive signal (before filtering) is applied to the audio monitor circuit. Thus, the craftsman can listen to the signals present on a circuit under test. During noise with tone measurements the holding tone presence is easily monitored via the built-in speaker.
LS1	loudspeaker	Allows signals on the circuit under test to be heard.
U1 – U5	Display LED readout	Provides readout of measurements results. **Impulse noise** display switch polls the "time left", "low," "medium", and "high" registers. "Time left" is displayed by two digits expressed in minutes with 1-minute resolution. The contents of the impulse noise counter registers are displayed by four digits expressed in "hits" with 1-hit resolution. Maximum counting rate is 7 pps. **Background noise** measurements are displayed by two digits expressed in dBrn with 1-dB resolution. Sampling rate is 2.5/sec. **Level** measurements are displayed by three digits expressed in dBm with 0.1-dB resolution. Sampling rate is 6/sec. **Frequency** measurements are displayed by four digits expressed in either Hz or kHz. Frequency display in Hz has a 1-Hz resolution and frequency display in kHz has a 10-Hz resolution. Sampling rate is 4/sec. Ranging in all measurements is automatic. An out of range condition is indicated by a blank display and a plus or a minus sign. The plus sign with a blank display indicates an overrange condition for a noise or tone signal. The minus sign with a blank display indicates an underrange condition for a noise or tone signal. A lighted KHZ indicator with a blank display indicates that input frequency is above the unit's accurate operating region.

Table 4—1. (Cont'd)

REFERENCE DESIGNATION	NOMENCLATURE	DESCRIPTION
CR1	kHz LED indicator	When lighted, indicates that the display is expressed in kHz. . .the set is in the frequency measurement mode. If the KHZ indicator is not lighted and the FUNCTION is set at FREQ, then the display is expressed in Hz. A lighted KHZ indicator with a blank display indicates that the input frequency is above the unit's accurate operating region. An erratically flashing KHZ indicator may occur if the input frequency varies above 99 kHz.
CR2	dBrn LED indicator	When lighted, indicates that the display is expressed in dBrn...the set is in one of the noise measurement modes other than impulse noise measurement.
CR3	DBM LED indicator	When lighted, indicates that the display is expressed in dBm...the set is in the tone level measurement mode.
CR4	IMPULSE LED indicator	When lighted, indicates that the display is expressed in hits or minutes...the set is in the impulse noise measurement mode.
IMPULSE NOISE		
S4	impulse noise display 4-position rotary switch	Polls the impulse noise register for display. TIME LEFT shows the time remaining. LOW shows the number of hits exceeding the lower threshold set by the LOW thumbwheel switch. MED shows the number of hits exceeding the medium threshold. Separation between thresholds set by SEP switch. HI shows the number of hits exceeding the high threshold. Separtion between thresholds set by SEP switch.
S16D1-D2	LOW THRESHOLD thumbwheel switches	Set the lower threshold level in dBrnC for impulse noise measurements.
S16D3	SEP. thumbwheel switch	Sets the separation in dB between thresholds at 2, 4, or 6 dB.
S16D4-D5	TIME thumbwheel switches	Set the test duration in minutes for impulse noise measurements. (Must be set at other than 00 for continuous impulse noise measurements.)

Table 4—1. (Cont'd)

REFERENCE DESIGNATION	NOMENCLATURE	DESCRIPTION
S17	IMPULSE COUNTER toggle switch	Controls impulse noise measurements. OFF/RESET - inhibits impulse noise measurement and resets the impulse noise test circuits. TIMED - enables impulse noise measurement for duration specified by TIME thumbwheel switches. CONT - enables impulse noise measurement on a continuous basis. . . for test durations longer than 99 minutes. Some time (any value) must be set on the TIME thumbwheel switches. NOTE To measure impulse noise, the FUNCTION switch must be set at one of the three noise positions (CKT, WITH TONE, or TO GND).
SEND		
S5	LEVEL DBM rotary switch	Selects the send level range in 10-dB steps. This switch operates as a coarse adjustment.
R2	LEVEL DBM potentiometer	Continuous control of the send level. The range of this control exceeds 13 dB. Thus the send level can be set anywhere between the present switch setting and 13 dB lower, with overlap at each end. The knob may be locked after setting. NOTE Always set the send signal level at the impedance of the circuit under test with both the send and receive impedances set at the same value (CAL SEND).
S6	FREQ HZ rotary switch	Selects one of four fixed frequencies or one of three frequency ranges for the send signal. The 1004 Hz signal can be used as a milliwatt signal or as a holding tone signal. The 404 Hz and 2804 Hz (together with 1004 Hz) are used to make attenuation distortion measurements. The 82 kHz can be used to test local loop cable pairs within a digital data system. The three frequency ranges cover the 35 Hz to 60 kHz band. The OFF position shuts down the send section. NOTE The FREQ HZ switch should be set at OFF when measuring impulse noise.

Table 4—1. (Cont'd)

REFERENCE DESIGNATION	NOMENCLATURE	DESCRIPTION
R1	FREQ HZ dual coarse/fine potentiometer	Sets the send frequency anywhere within the selected range with some overlap at each end. When setting the frequency with the FREQ HZ control, always pass by the desired frequency to coarse tune, then reverse direction to fine tune. The direction of tuning is unimportant. Coarse tuning should be done slowly to avoid excessive overshoot. The knob may be locked after adjustment.
R158	recessed screw driver adjustment potentiometer	Precisely sets the 2804-Hz fixed frequency. 404-Hz and 1004-Hz frequencies should track accordingly.
DIAL AND HOLD GROUP		
J10,J11	DIAL square posts	Provides a quick and convenient way to connect a lineman's handset for dialing through the set.
S3	HOLD A + B toggle switch	When ON, connects a hold coil across the tip and ring of an input/output line if the SEND IMPEDANCE switch is not set at DIAL A or DIAL B.
S7	SEND IMPEDANCE (DIAL) rotary switch, outer knob	Selects the set's output impedance and chooses the output line (A or B) on which dialing will be sent. When SEND IMPEDANCE (DIAL) switch is set at either DIAL A or DIAL B, the test set has a 600-ohm input/output impedance.
IMPEDANCE/LINE SELECT		
J1,J4	Lines A and B 310 jacks	Enable connection of external circuits to test set.
J2,J3 and J5,J6	Lines A and B T and R binding posts	Provide alternate way to connect external circuits to the set.
S7	RECEIVE IMPEDANCE rotary switch, inner knob	Selects the set's input impedance.

Table 4—1. (Cont'd)

REFERENCE DESIGNATION	NOMENCLATURE	DESCRIPTION
S8	LINE SELECT rotary switch	Assigns line A or line B as the send line and the other line (B or A) as the receive line. Permits changing the send and receive directions without disconnecting external circuits. NOTE When testing with different send and receive impedances, the IMPEDANCE switches must be repositioned if the line A and line B assignment is exchanged. When in CAL SEND position, the send signal goes directly to the receive section. This permits setting the level and frequency of the send signal without having to detach any external circuits connected to the set. NOTE Always adjust the send signal level at the impedance of the outgoing circuit under test with both the send and receive impedances set at the same value. NOTE When setting the send level (LINE SELECT switch set at CAL SEND), the TERM/BRDG switch should be set at TERM; otherwise, the BRDG position will insert a 6-dB error when adjusting the send level.
DS1	CAL SEND indicator	When lighted indicates that LINE SELECT switch is in CAL SEND position.
J7,J8	Lines A and B; SL pin jacks	Provides access to the sleeve leads of the input/output lines. The sleeve leads are isolated and floating with respect to chassis ground. Control can be exercised via these jacks when testing on sleeve-supervised circuits.
S2	TERM/BRDG toggle switch	Determines whether the receive section terminates or bridges across the circuit under test. The IMPEDANCE (DIAL) should always be set at the impedance of the circuit under test regardless of the TERM/BRDG switch position.

Table 4—1. (Cont'd)

REFERENCE DESIGNATION	NOMENCLATURE	DESCRIPTION
RECEIVE GROUP		
S9	FUNCTION rotary switch	Selects the measuring modes. There are one level, one frequency, and three noise measuring modes. **Level mode:** tone level measurements can be made in the frequency range of 35 Hz to 85 kHz over a dynamic range of −70 dBm to +15 dBm. A 200 Hz to 10 kHz bandpass filter can be inserted to suppress low and/or high frequency noise. **Frequency mode:** tone frequency measurements can be made from 20 Hz to 85 kHz. Tone level and frequency measurements can be used for determining loss and attenuation distortion on message trunks and data services. A 200 Hz to 10 kHz bandpass filter can be inserted to suppress low and/or high frequency noise. **Circuit noise mode:** Metallic (balanced) noise can be measured with both tip and ring leads isolated from earth ground. Any one of four standard and one optional weighting filters may be used. Measurement range for the circuit noise mode is 0 dBrn to 85 dBrn for 600-ohm and 900-ohm circuits and 10 dBrn to 85 dBrn for 135-ohm circuits. **Noise with tone mode:** Noise with tone measurements may be used to give a measure of noise encountered by a continuous data signal, or the noise a listener would hear during a speech burst. In noise with tone mode a sharp 1010-Hz notch filter is switched into the receive section. The notch filter eliminates any tone between 995-Hz and 1025-Hz present on a circuit under test. The measurement range for the noise with tone mode is 10 dBrn to 85 dBrn for 600-ohm to 900-ohm circuits and 20 dBrn to 85 dBrn for 135-ohm circuits. Noise with tone or circuit noise measurements can be used to determine signal to noise ratio on a circuit. **Noise to ground mode:** In this mode the noise level between two sides of a balanced line can be measured. The results are read directly as true values between 50 dBrn and 135 dBrn, with no correction. NOTE Always connect the test front panel GND binding post to earth ground (or system ground) when measuring noise to ground.

Table 4—1. (Cont'd)

REFERENCE DESIGNATION	NOMENCLATURE	DESCRIPTION
S10	WEIGHTING five-position rotary switch	Selects one of five weighting filters for noise measurements. The weighting filters are: C-message, 3-kHz flat, 15-kHz flat, program, and 50-kb/s. **C-message:** The C-message filter has a frequency response which simulates the effects of noise on the human ear as received on a type 500 set. C-message weighting can be used to evaluate the effects of noise on voice-grade data circuits. Figure 2—1 shows the frequency response of a C-message filter. **3 kHz Flat:** The 3-kHz flat weighting filter is used on voice frequency circuits when investigating low frequency noise, such as power induction. Figure 2—2 shows the 3-kHz flat filter frequency response. **15 kHz Flat:** The 15-kHz flat filter is used for unweighted measurements of noise on radio and television studio transmitter and studio-remote audio links. Figure 2—3 shows the 15-kHz flat filter frequency response. **Program:** The program filter is used for weighted measurements of noise on radio and television studio-transmitter and studio-remote audio links. Figure 2—4 shows the program filter frequency response. **50-kb/s:** The 50-kb/s filter is used for measurements of noise on digital data circuits. Figure 2—5 shows the 50-kb/s filter frequency response.
S11	MON SEND FREQ momentary action pushbutton switch	Applies a portion of the send signal directly into the receive section for frequency measurement. This feature provides a convenient way to adjust the frequency without interrupting the line connection.
S12	0.2-10 KHZ B.P. FILTER momentary action pushbutton switch	Inserts a bandpass filter in the receive section when held pressed if the level tone or frequency measuring mode has been selected. Filter attenuates low and high frequency noise present on the circuit under test. Figure 2—6 shows the bandpass filter frequency response.
S13	DAMPING momentary action pushbutton switch	Dampens the noise measurement circuit so that the display shows the long-term average noise value.
S14	FREQ momentary action pushbutton switch	Changes the noise measuring mode into a frequency measuring mode, but leaves the noise weighting filter in the receive signal path. This feature counts and displays the frequency of the predominant signal present in the filter-weighted input noise spectrum. The single frequency readout in conjunction with the audio monitor can help pinpoint such noise problems as: 1. Leaky SF; 2. 60 Hz and its harmonics; 3. Spurious network tones.

Table 4—1. (Cont'd)

REFERENCE DESIGNATION	NOMENCLATURE	DESCRIPTION
POWER		
S1	POWER-ON	Controls application of power to the set. If the set is connected to an ac power source, internal regulators supply the necessary dc voltages.
J9	GND binding posts	Provides method of connecting the set to a ground. **WARNING** **To ensure operator protection, connect the front panel GND terminal to earth ground when operating in the battery mode.**
REAR PANEL		
S15	115/230 switch	Configures the set for 115 or 230 Vac operation.
F4,F5	fuses	Protects set against excessive input current. Use a 0.3 Amp slow-blow fuse for 115 Vac operation. Use a 0.2 Amp slow-blow fuse for 230 Vac operation.
J15	Battery jack	Connects set to optional battery pack.
J12	Power jack	Connects set to an ac power source.

4.23 IMPULSE NOISE MEASUREMENT PROCEDURE

1. Connect circuit under test to the 310 jack or to the T and R binding posts of the desired input line (line A or B).

2. Set LINE SELECT switch at SEND A/RCV B or at SEND B/RCV A, depending on the input connections made in step 1.

3. Set RECEIVE and SEND IMPEDANCE (DIAL) switches at the circuit-under-test impedance(s).

4. Set IMPULSE COUNTER switch at OFF/RESET.

5. Set line TERM/BRDG switch as required.

6. Set FUNCTION switch at a NOISE measurement position as required.

NOTE

Impulse noise measurements are normally made with a 1004-Hz holding tone present on the circuit-under-test at typical transmitted level of −13 to −16 dBm. For such measurements, the receiving Model 4002 FUNCTION switch should be set at WITH TONE position.

For special cases where impulse measurements are required with no holding tone present, set FUNCTION switch at CKT position. If impulse measurements are ever required on a noise to ground (unbalanced) basis, set FUNCTION switch at TO GND position.

7. Set WEIGHTING switch for the required noise filter (C-MSG or 3 KHZ FLAT or 15 KHZ FLAT or PRGM or 50 kb/s). Standards relate to C-MSG and 50 kb/s filters.

8. Set impulse noise display switch at TIME LEFT.

9. Set LOW THRESHOLD thumbwheel switches for required lower threshold level.

10. Set SEP thumbwheel switch for required separation between thresholds.

11. Set TIME thumbwheel switches for desired duration of impulse noise test.

NOTE

If a continuous impulse noise test is to be made, the TIME thumbwheel must be set at some value other than 00.

12. To start test, set IMPULSE COUNTER switch at TIMED or at CONT.

13. After a timed impulse test is completed (display reads 00), use the impulse noise display switch to show the contents of the LOW, MED, and HI threshold counters.

4.24 TONE LEVEL MEASUREMENT PROCEDURE

1. Connect circuit under test to the 310 jack or to the T and R binding posts of the desired input (line A or B).

2. Set LINE SELECT switch at SEND A/RVC B or at SEND B/RCV A, depending on the input connections made in step 1.

3. Set RECEIVE and SEND IMPEDANCE (DIAL) switches at the circuit-under-test impedance(s).

4. Set line TERM/BRDG switch as desired.

5. Set FUNCTION switch at LEVEL.

6. Read tone level in dBm on the digital display.

7. To measure level without influence from low and/or high frequency noise, hold 0.2-10 kHZ B.P. FILTER pushbutton pressed and read digital display.

NOTE

A blank display with a plus sign indicates the input levels exceed +15 dBm. A blank display with a minus sign indicates the input level is less than −70 dBm.

NOTE

There exists approximately 2 dB of hysteresis at both ends. Once blanked, it is necessary to increase or decrease (whichever is the case) the input signal level for the display to reappear.

4.25 FREQUENCY MEASUREMENT PROCEDURE

1. Connect circuit under test to the 310 jack or to the T and R binding posts of the desired input (line A or B).

2. Set LINE SELECT switch at SEND A/RCV B or at SEND B/RCV A, depending on the input connections made in step 1.

3. Set RECEIVE and SEND IMPEDANCE (DIAL) switches at the circuit-under-test impedance.

4. Set line TERM/BRDG switch as desired.

5. Set FUNCTION switch at FREQ.

6. Read frequency in Hz or kHz on the digital display. The KHZ indicator is lighted to show kHz range.

NOTE

The kHz range has a 10 Hz resolution, and the HZ range has a 1 Hz resolution.

NOTE

A blanked display with the KHZ indicator lighted shows that the input frequency is too high for the set to measure.

4.26 SEND SECTION OPERATING PROCEDURE

1. Connect circuit under test to the 310 jack or to the T and R binding posts of the desired input (line A or B).

2. Set LINE SELECT switch at CAL SEND.

3. Set both SEND and RECEIVE IMPEDANCE (DIAL) switches at the circuit-under-test impedance(s).

4. Set FUNCTION switch at FREQ.

5. Set FREQ HZ switch at the desired frequency range or at a fixed frequency.

6. If a frequency range was selected, adjust the FREQ HZ control to obtain the desired frequency reading on the display. Coarse tune slowly past the desired frequency and then reverse to fine tune. Lock knob in position.

7. Set FUNCTION switch at LEVEL.

8. Set LEVEL DBM switch to nearest higher 10 dB setting for the desired send level. Example: Set LEVEL DBM switch at the −10 for a −14 dBm desired output level.

9. Adjust the output to the desired level with LEVEL DBM control. Lock knob in position.

10. Set LINE SELECT switch at SEND A/RCV B or at SEND B/RCV A, depending on the connection made in step 1. Send section signal is now applied to circuit under test.

SECTION 5

THEORY OF OPERATION

5.1 INTRODUCTION

5.2 Figure 7–1 identifies six major sections of the Model 4002 Test Set.

- The **send** section generates a test tone easily set at precise frequencies and levels. The tone is supplied to the circuit under test via the input-output section.

- The **input/output** (I/O) section routes send section outputs to the Line A or B part while routing incoming signals to the receive section. The outgoing dial signaling circuit and the incoming line holding circuit are part of the I/O section.

- The **receive** section adjusts incoming signal levels to the dynamic range of the measure section. This section includes automatic ranging, amplification, and selectable filtering circuits. Detected signals which accurately describe incoming signal characteristics are supplied by the receive section to the measure sections. Out-of-range conditions which would void measurement results are detected.

- The **level and frequency** measurement section converts analog inputs from the receive section to binary-coded-decimal (BCD) data in appropriate units (Hz, kHz, dBm, dBrn). Special measurement conditions are detected. These conditions flag the display section, which modifies the display as is appropriate for the condition.

- The **impulse noise measurement** section converts an analog output of the receiver to BCD counts of incidence of noise impulses which exceeds one or more of three preset dBrn thresholds. This section also includes the down-counting presettable time-left counter which controls the data-taking interval.

- The **display** section gates operator-selected BCD data to the digit display. This section also controls the four LED indicators to the right of the digit display. Display blanking inhibits leading zeros and inhibits digit display in presence of an out-of-range condition.

5.3 GENERAL BLOCK DIAGRAM

5.4 Paragraphs 5.5 through 5.36 refer to Figure 7–1, the Model 4002 general block diagram.

5.5 SEND SECTION

5.6 The sine-wave oscillator supplies signals over the range of 35 Hz to 60 kHz. Fixed frequencies 404 Hz, 1002 Hz, 2804 Hz and 82 kHz can be selected with FREQ Hz switch S6. Ranges 35 to 375 Hz, 0.375 to 4.5 kHz and 4.5 to 60 kHz can be selected with the same switch. FREQ Hz control R1 sets the operating frequency in the selected band.

5.7 The output level control amplifies the oscillator output. The send section supplies an accurate level in the range of −50 to +13 dBm to the circuit under test. LEVEL DBM control R2 varies the output level through the 10-dB range selected by LEVEL DBM switch S5. The output level is accurate with 135-, 600-, and 900-ohm loads. SEND IMPEDANCE switch S7 matches the send section output circuit to loads having these impedances.

5.8 A sample of the send section output tone is supplied to the receive section. Actuation of MON SEND FREQ S11 selects the frequency measurement mode and connects the sample to the receiver. This permits tone frequency setting to the accuracy of the measurement section (to the nearest Hz to 9999 Hz; to the nearest 10 Hz to 60 kHz).

5.9 INPUT-OUTPUT SECTION

5.10 The input to the I/O section from the send section can be connected to the LINE A or B port by LINE SELECT switch S8. Also, dialing signals supplied by an external source can be connected to LINE A or B (SEND IMPEDANCE switch S7). The send signal is interrupted with DIAL A or B enabled. When LINE SELECT switch S8 is at CAL SEND and the test set is in the LEVEL mode, it is possible to set the output level to the accuracy of the measurement section.

5.11 An input from the circuit under test via LINE A or B port is switched to the receive section by LINE SELECT switch S8. Holding coils are inserted across the incoming circuit by HOLD A & B switch S3.

5.12 RECEIVE SECTION

5.13 The receive section input circuit impedance can be set at 135, 600, or 900 ohms (REC IMPEDANCE switch S7). The input circuit under test can be terminated or bridged as determined by TERM/BRDG switch S2. Noise-to-ground measurements are made through a 50-dB pad rather than through the input transformer.

5.14 The active circuits in the receive section and the level measurement circuits operate over a 14-dB range (−48 dBm to −62 dBm input equivalent in most ranges). The receiver uses an input attenuator to place "slices" of the over-all input range of 85 dB within the 14-dB window. Also, the attenuator is used to place "slices" of the 101-dB over-all range in the impulse noise measurement mode within the 22-dB window of the impulse noise measurement circuits. The attenuator has a range of 0-60 dB in 10-dB steps. The attenuator is set automatically for all measurements except impulse noise.

5.15 Measurements of noise level with a 1004-Hz tone present are made by notching out the tone. When the FUNCTION switch is set at WITH TONE, a 1010-Hz notch filter is inserted in series with the signal path.

5.16 A 0.2- to 10-kHz active bandpass filter can be switched into the signal path during tone level and frequency measurements. This filter suppresses low- and high-frequency noise. The bandpass of the circuit during these measurements without the filter is 35 Hz to 85 kHz. When in any noise mode, one of the five weighting filter identified in Figure 7−1 can be inserted in series with the signal path.

5.17 One output of the filter-amplifier connects to the impulse noise amplifier-attenuator-detector. This circuit detects the peak level of impulse noise spikes. Impulse noise is detected over a 101-dB range (10 to 111 dBrn). LOW THRESHOLD switch S16D1 (tens of dB) sets the receiver input attenuator over a 60-dB range and the impulse path attenuator over a 20-dB range (80 dB total). LOW THRESHOLD switch S16D2 (units of dB) sets an impulse path circuit over an additional 10-dB range (90-dB combined range). (The impulse noise measure section operates through an additional 12-dB range.)

5.18 A second output of the filter-amplifier circuit (Vac) feed the frequency measurement circuit and a rectifier-filter. The filter output is related to the average value of Vac in the tone level and frequency measurement modes. When in noise measurement modes, the output is related to the rms value of Vac.

5.19 The damping circuit is an active long-time-constant network. When enabled, this circuit suppresses short-term variations while leaving long-term variations unaffected. This circuit, activated by momentary action DAMPING switch S13, is used only during noise measurements other than impulse noise. The output of DAMPING switch S13 feeds the receiver auto-ranging circuit and circuits in the level and frequency measurement section.

5.20 The auto-ranging circuit monitors the detector output voltage. This circuit produces range selection signals which control the 0-60 dB attenuator such that the detector output is brought to within the test set's 14-dB measurement window (17 dB in the highest range, R7). To accomplish this, the auto-ranging circuit determines whether the detector output is below, within, or over the current measurement range. The attenuator can be switched in either direction. When the detector output remains below the low limit after selecting the lowest range or remains above the upper limit after selecting the highest limit, level measurements are disabled (the ENABLE signal) and the digit display is blanked. Also, inhibits frequency measurements.

5.21 The ranging control select circuit substitutes the manual range selection controls for the auto range selection controls when in impulse noise measurement mode.

5.22 LEVEL AND FREQUENCY MEASUREMENT SECTION

5.23 The circuits in this section measure frequency (in Hz or kHz), tone level, circuit noise, noise with tone, and noise to ground. Level measurements are made on the receiver VDET output. Frequency measurements are made on the receiver square-wave output.

5.24 The analog-to-digital (A-D) converter is enabled when the receiver auto-ranging has settled at a point which yields a receiver output within the dynamic range of the measurement circuits. The receiver analog output VDET is compared with a logarithmic reference. The result is a pulse having a width determined by signal level relative to the upper limit of the selected receiver range. This pulse gates the 102.4 kHz clock. Each gated clock represents a 0.01-dB increment. The input is sampled 375 times per minute in the tone level measurements and 150 times per minute in noise measurements.

5.25 The counter and storage circuits include a five-stage counter. When measuring level, the lowest order stage counts in 0.01-dB increments; the highest-order stage is in 100-dB increments. These stages count each burst from the A-D converter. The contents of the four highest-order stages are available to the display section. When the A-D converter completes a sample, the end-of-measure (EOM) signal is sent to the measurement control circuit. The circuit first produces the XFR, then the PE signal. The XFR signal moves counter contents into storage. The PE signal enters a starting count into the counter.

5.26 The purpose of the stuffing logic and the need for a starting count are best made evident by considering a typical tone level measurement. Given a line input of −25 dBm, the attenuator will be set at 30 dB by the receiver auto-ranging circuit. The attenuator output (−55 dBm) will thus lie in the normal receive section input equivalent range of −48 to −62 dBm. The signal level is 7 dB below the upper end of this range; this is the figure measured by the A-D converter. It is obvious that −7 dBm would not be a correct result to display. With the attenuator at 30 dB in the tone power level mode, the stuffing logic enters 18 dB as a starting count. The counter accumulates an additional count of 7 dB to produce a total of 25 dB (the display shows −25 dBm). The stuffed number varies with mode and the auto-ranging setting point. (In several measurement conditions, it is necessary to stuff first one and then an alternate number for a given range. The CARRY signal from the counter controls this event.)

5.27 The frequency measurement circuit includes a phase-locked loop. A voltage-controlled oscillator is locked at a frequency four times the detected frequency. The VCO is gated by a 250-millisecond gate to produce a clock for the counter representing one clock per cycle of the input frequency. Frequency counts accumulate in four highest order stages when the input frequency is below 10-kHz (1-Hz resolution) and in the five stages if the input frequency is above 9999 Hz. The frequency count is displayed as a 4-digit value. Range switching is automatic. The range extends to 60 kHz. Four measurements are made per second. The frequency measurement circuit produces FEOM, used by the measurement control to produce XFR and PE. The stuffing logic inserts 00000 since frequency counts are not referenced.

5.28 IMPULSE NOISE MEASUREMENT SECTION

5.29 The impulse noise measurement section includes counters for registering impulse noise events at three threshold levels. Date accumulation time is controlled by a fourth counter, which can be preset for a 1- to 99-minute interval. Control logic also permits continuous collection of data.

5.30 The receiver amplifier-attenuator-detector output is compared with three references. The lowest reference represents the setting of LOW THRESHOLD S16D1 and S16D2. The two higher references are separated by 2, 4, or 6 dB from the low reference as set by SEP switch S16D3. A pulse appears at a comparator output when detected impulse noise exceeds its reference. The HI LEVEL, MED LEVEL, and LOW LEVEL pulses are registered separately by three counters. Each counter input is masked for 140 milliseconds after an event. The maximum clock rate is thus 7 events per second. Counter contents are frozen upon expiration of the preset collection interval (unless IMPULSE COUNTER switch S17 is at CONT, in which condition collection is continuous).

5.31 The time-left counter is preset to the desired collection interval by setting TIME switches S16D4 and S16D5. The time-left divider produces a clock having a one-minute period. The counter decrements from the preset number. When the count reaches zero, the time-left and event counters freeze.

5.32 DISPLAY SECTION

5.33 The display includes a four-digit segment display with a polarity indicator and four individual LED indicators (DBM, KHZ, dBrn, and IMPULSE). The display section gathers BCD data from the active measurement section one digit at a time (from highest to lowest order, identified as A through D).

5.34 The data output control supplies a four-phase clock SCAN DIGITS A-D. The digit gate passes level, frequency, and noise data from the level and frequency measurement section. The impulse counter digit gates pass low, medium, or high event counts, whichever are selected by switch S4 in impulse noise. The time-left digit gate passes time-left data when selected by switch S4 during impulse noise measurement. Each gate BCD digit is decoded to serve the seven-segment displays. The display selection and blanking control uses SCAN DIGITS A-D to produce the four sequential SELECT DIGIT A-D gates, which enable the four digit indicators from left to right. The digit display is updated 450 times per second.

5.35 The display selection and blanking control tests data for leading zeros and produces blanking gates to inhibit their appearance on the display. Also, carry outputs from the counter and storage circuit in the

power and frequency measurement section are tested in the frequency mode to provide frequency autoranging. The kHz output is produced when the count exceeds 9999 Hz. The four LED indicators are controlled as follows:

- ☐ DBM = level
- ☐ KHZ = frequency greater than 9999 Hz
- ☐ dBrn = circuit noise, noise with tone, noise to ground
- ☐ IMPULSE = impulse noise

5.36 Polarity indications in the presence of out-of-range conditions are as follows:

- ☐ Plus: Receiver auto-ranging produces an over-range indication in level or noise measurement mode.
- ☐ Minus:
  - Receiver auto-ranging produces an under-range indication in level or noise measurement mode.
  - Noise level is less than 0 dBrn in circuit noise or noise with tone measurements mode.

The digit indicators are blanked in these conditions. Also, the digit display is blanked when the input frequency is beyond the upper measurement limit during frequency measurements.

5.37 SEND SECTION FUNCTIONAL DIAGRAM (FIGURE 7—2)

5.38 Triangular-wave generator U20-U23 supplies symmetrical ramps to the sine-wave converter. The generator operates at one of four fixed frequencies or at a frequency within one of three ranges. The triangular wave is converted to a sine wave by CR22-CR37, controlled by U24, U25 and associated voltage dividers. Calibration potentiomenter R158 sets fixed frequencies 404, 1004, and 2804 Hz. Six other adjustments effect output distortion.

- ☐ SYMMETRY (R161): This adjustment equalizes the negative and positive slope intervals. Any difference in the intervals constitutes distortion.
- ☐ LEVEL (R166): This adjustment affects distortion at or near output voltage positive and negative peaks.
- ☐ FREQ COMP (R168): This adjustment has the same effect as R166 but it is in the circuit only in the 4.5- to 60-kHz range.
- ☐ CROSSOVER (R219): This adjustment affects both positive and negative voltages near zero volts.
- ☐ −BIAS (R170): This adjustment affects the waveshape of negative half cycles from the converter.
- ☐ +BIAS (R189): This adjustment affects the waveshape of positive half cycles from the converter.

The converter output is buffered by U26 (3.8 dB gain). Frequency components above about 80 kHz are attenuated by low-pass filter U27. The filter output is connected to the monitor circuit through the receive section to allow setting output frequency without patching LINE ports. The filter output also feeds a step attenuator.

5.39 Step attenuator R230-R238 and the 20-dB attenuator, controlled by LEVEL DBM switch S5, provide six 10-dB power ranges. The gain of the output amplifier can be varied over a 12-dB range by LEVEL DBM potentiometer R2. The 12-dB span allows overlap between ranges.

5.40 The send section output level specifications apply to 135-, 600-, and 900-ohm circuits. To preserve the integrity of the LEVEL DBM switch markings, it is necessary to supply an appropriate signal voltage to each load impedance. SEND IMPEDANCE switch S7 controls the gain of the output amplifier for this purpose. Also, the IMPEDANCE switch connects the output transformer A5T1 secondaries in series (600 or 900 ohms) or in parallel (135 ohms) to ease impedance matching. The analog board output network and the I/O board impedance matching network also influence impedance matching.

5.41 The balanced capacitively-coupled tip/ring output is connected to the I/O section. See Figure 7—3 and Paragraph 5.59.

5.42 SEND SECTION DETAILED DISCUSSION

5.43 TRIANGULAR-WAVE GENERATOR (FIGURE 7—22)

5.44 The integrator output is a ramp voltage. The comparator monitors the ramp voltage and switches

output state when the ramp voltage at its positive input equals the voltage applied to its negative input by the first inverter. The change in comparator output state causes the first and second inverters to change output states. The resulting polarity change at the second inverter output forces a polarity change in the slope of the integrator ramp voltage. Thus, the integrator output consists of positive and negative ramps which makeup the triangular waveform. Potentiomenter R161 adjusts integrator balance to set waveform symmetry.

5.45 The ramp voltage slope, which determines frequency, depends on the integration rc time constant. FREQ switch S5 selects the resistance and capacitance to set the basic integration time constant. FREQ control R2 modifies the time constant to control the frequency for the first three FREQ switch positions. Potentiometer R158 modifies the time constant for the last three FREQ switch positions, but its frequency adjustment range is very small. Therefore, the first three FREQ switch positions are tunable frequency bands and the last three switch positions are fixed frequencies. The triangular waveform goes to the diode function generator.

5.46 DIODE FUNCTION GENERATOR AND BUFFER (FIGURE 7–22)

5.47 The diode function generator is comprised of bias buffers U24 and U25, diodes CR22-CR37, resistors R173-R189 and R192-R221. The triangle-to-sine wave transfer characteristic is obtained via a non-linear resistance produced by the network of resistors and diodes (operating as voltage controlled switches). Each diode conducts whenever the triangular-wave voltage (to which one side of each diode is connected) reaches the bias voltage present on the other side of the diode.

5.48 Then the triangle wave is at zero volts all the diode switches are open and the signal appears unchanged at the input of buffer amplifier U26. As the signal increases in the positive direction it reaches the bias voltage point present on the cathode of diode CR37. At this point, diode switch CR37 conducts. The anode of diode CR37 is now clamped at the bias present on its cathode. As the signal continues to increase, diode switch CR35 conducts with its anode clamped at the bias voltage present on its cathode. This process continues until the signal reaches its maximum value and diodes CR23 CR37 (odd numbers only) all conduct.

5.49 The net result is that resistor string R207-R221 presents an increasing load to the triangular wave through resistors R165 and R166. The signal appearing at the buffer amplifier input varies in a close simulation of a sine wave. As the triangular wave decreases from maximum value the process reverses and diode switches CR23-CR37 (odd numbers only) open up one at a time. The negative portion of the triangle wave is then handled in a similiar manner by diode switches CR22-CR36 (even numbers only).

5.50 Bias buffers U24 and U25 offset and isolate the bias reference voltages from the loading effects of the resistor string. Potentiomenters R170 and R189 adjust the negative and positive bias voltages and have pronounced effects on the sine wave shape. Potentiometer R166 is set to achieve the minimum voltage at which diodes CR23 and CR22 have the same degree of effect on simulation as the lower threshold diodes. Thus, this control affects distortion at or near output voltage peaks. Potentiometer R168 has the same effect but is in the circuit only when the 4.5- 60-kHz range is selected. Potentiometer R219 has the most noticeable influence on the circuit when only diode CR36 or CR37 is closed. This potentiometer is set to achieve minimum distortion in the crossover region.

5.51 Buffer U26 has a gain of 3.8 dB. The lowpass filter consists of a single-pole filter (R224, C81) in series with infinite-gain multiple-feedback active filter U27. The complete lowpass filter is a 3-pole design with an 80-kHz cut-off frequency. The filter attenuates high-frequency harmonics from the buffer output signal.

5.52 OUTPUT CIRCUIT (FIGURE 7–22, 7–26)

5.53 The filtered sine wave passes through the output circuit, which sets the sine wave output level. Step attenuator R230-R238 is a tapped string of resistors that has a minimum of 14-dB attenuation. The step attenuator (in conjunction with 20-dB L-attenuator R247, R248, and R278) decreases the sine wave level in 10-dB steps for succeding positions of LEVEL DBM switch S5.

5.54 The output amplifier, located between the step and L-type attenuators, consists of IC operational amplifier U28 and emitter followers Q40 and Q41. The operational amplifier and the emitter followers operate as one non-inverting amplifier. The emitter followers each conduct on alternate half-cycles to boost the operational amplifier's current drive. Diodes CR38-CR40 minimize crossover distortion. Diodes CR41 and CR42 limit the output to 24 volts peak-to-peak.

5.55 Two elements control the amplifier gain. LEVEL DBM control R2 adjusts the amplifier gain over a range greater than 11 dB. IMPEDANCE switch S7 connects different feedback resistors to shift the gain range. For the 900-ohm position, the gain can be varied between 15.9 and 4.5 dB. in the 600-ohm position the gain can be set between 17.7 and 5.4 dB. In the 135-ohm position the gain is adjustable between 19.7 and 6.6 dB.

5.56 The output impedance network is comprised of resistors R249-R252, capacitors C91-C92, thermistor RT1, and gas protector E1. The thermistor maintains the impedance of the output network constant with changing temperature. The gas protector prevents voltage surges from damaging the test set. The output impedance network in series with the impedance of the L-attenuator has an output impedance of 90 ohms. This impedance is reflected on the output side of transformer A5T1 as 900 ohms for the 900- and 600-ohm positions of the IMPEDANCE SWITCH. In the 135-ohms position, the reflected impedance is 225-ohms. Capacitors C91 and C92 provide frequency compensation.

5.57 Output transformer A5T1 has a 1:10 impedance ratio when the IMPEDANCE switch is set at 900 or 600. The impedance ratio changes to 1:2.5 for the 135-ohm position. Therefore, the transformer functions as a step-up transformer with a 10-dB voltage gain for 600- and 900-ohm switch positions and a 4-dB voltage gain for the 135-ohm position.

5.58 See Figure 7—26. The impedance matching network changes the reflected impedance to the selected output impedance. In 900-ohm position of the IMPEDANCE switch, the 900-ohm reflected impedance appears as the test set's output impedance. In 600-ohm position, resistor R29 (in parallel with the 900-ohm reflected impedance) changes the test set output impedance to 600 ohms. In 135-ohm position, resistors R30 and R31 lower the 225-ohm reflected impedance to give the test set a 135-ohm output impedance. Capacitors C11 through C15 provide matching for optimum return loss at each of the output impedances.

5.59 INPUT/OUTPUT SECTION FUNCTIONAL DIAGRAM (FIGURE 7—3)

5.60 Input/output switching is done on circuit board A5. LINE SELECT switch S8 connects the send and receive sections to LINE A and LINE B jacks J1-J6. In the CAL SEND position, the send section is connected to the receive section, leaving LINE A and B jacks disconnected. The CAL SEND feature allows use of the receive and level measurement sections to read output level without disconnecting the circuit under test from the LINE jacks.

5.61 Hold coils L1 and L2 are connected across lines B and A, respectively, when HOLD A & B S3 is ON. Sections C and D of SEND IMPEDANCE switch S1 disconnected the send section from the sending line jack when DIAL A or DIAL B is selected. At the same time, the square DIAL jacks are connected to the sending LINE jack.

5.62 See Figure 7—26 for the schematic diagram of the input/output board.

5.63 RECEIVE SECTION FUNCTIONAL DIAGRAM (FIGURE 7—4)

5.64 The receive section includes circuits on five circuit boards.

- ☐ Input/output board (input circuit)
- ☐ Analog board (step attenuator, amplifiers, filters, analog output circuits)
- ☐ Digital board (auto-ranging, damping, square-wave converter)
- ☐ Display driver board (impulse noise amplifier, attenuator, detector)
- ☐ Logic board B (ranging selector)

5.65 The circuit under test tip and ring leads are bridged resistively for noise to ground measurements, transformer-bridged (for all other measurements) with S2 set at BRDG switch or terminated in 135, 600, or 900 ohms (all measurements except noise to ground) with switch S2 set at TERM.

- ☐ Noise to ground - Resistor R27 and R28 are connected through S9A, C7, and C8 to A5R13 and A4R2. This network forms a 50-dB pad with noise to ground selected. Section A of S9 disconnects T2 primaries from C7 and C8.
- ☐ Transformer bridging - The primaries of T2 are connected in series through blocking capacitors C7 and C8. With the TERM/BRDG switch S2 at BRDG, the primaries are disconnected from the terminating impedances. The high-impedance (greater than 25 kohms at 1000 Hz) primaries bridge the circuit under test with this setting.
- ☐ Input termination - With S2 at TERM (and FUNCTION switch S9 at any position other than noise to ground), a terminating impedance (135, 600, or 900 ohms as selected with REC IMPEDANCE switch S7) is placed across each primary of T2.

5.66 The unbalanced transformer output connects through R9 (or R9 in parallel with R10 with S2 at TERM) to QD12 on the analog board. Section B of S9 selects this output (any position other than noise to ground) or the 50-dB pad output (noise to ground).

5.67 The 0-60 dB step attenuator is set by seven ranging signals. The ranging signals originate from the receiver auto-ranging circuit (any mode other than impulse noise) or the manually controlled 10-dB thumbwheel switch S16D1 (impulse noise switch S16 is part of A8). Range select circuit on logic board B chooses the ranging signal source. Ranging signals are designated R0 through R7. The R0 signal designates the lowest range, not used specifically by the step attenuator. The R1 through R7 signals specify the six highest ranges, and correspond to the 0-dB through 60-dB settings of the attenuator.

5.68 The step attenuator output drives amplifier U4 directly in all but one measurement mode. Amplifier U1 and notch filter U13 are inserted in the signal path for noise with tone measurements. The 6-dB gain of U1 offsets the 6-dB insertion loss of U13. The notch filter offers 50 dB attenuation at 1010 Hz. Audio amplifier U2/U3 compresses input amplitude to yield loudspeaker levels that vary little with input signal level.

5.69 Incoming signals produce voltages which are amplified linearly and detected logarithmically for level measurements. An input signal of a given power produces different voltages with different line impedances. To compensate for this, the receive section gain is changed in accordance with the selected input impedance. Measurements are normalized to 900-ohm circuits. The gain of amplifiers U4 and U7 is about 30 dB with 900 ohms selected (about 11.2 and 18.7 dB, respectively). When 600-ohm impedance is selected, the 1.76-dB differential at the input circuit is offset by a gain of about 31.7 dB (11.2 dB and 20.54 in U4 and U7, respectively). The 8.24 dB differential with 135 ohms selected is offset by setting gains of 19.4 dB and 18.7 dB in U4 and U7, respectively.

5.70 Low-pass filter L1-C102 attenuates input frequencies above the measurement limit (65 kHz). Section D of S9 enables WEIGHTING switch S10 and the related filters in any noise position. The filters control the spectrum over which noise measurements are made.

- C-MSG: Bandpass; standard characteristics
- 3-kHz FLAT: Low-pass; flat to about 2 kHz; down about 3 dB at 3 kHz
- 15-kHz FLAT: Low-pass, flat to about 7 kHz, down about 12 dB at 15 kHz
- Program: Bandpass; see Section 2
- 50-kb/s: Low-pass; see Section 2

In level and frequency measurement modes, the signal is coupled directly to U7 (BP FILTER switch S12 not activated) or through the 200 Hz to 10 kHz filter (S12 activated). The filter attenuates noise outside of the bandpass.

5.71 The output of U7 is limited at about 1.4 volts peak-to-peak by diodes CR43 and CR44. Limiting does not occur within the power measurement window. This limited signal drives U8 and impulse noise circuitry on display driver board A8. Amplifier U8 offers 17-dB gain in level and frequency measurement by 10-dB in the lowest receiver range (RO). The stage has 37 dB gain in noise measurement modes, increased by 10 dB in the lowest receiver range. The 20-dB gain difference between noise and level brings the noise measurement window in coincidence with the level measurement window. Low-pass filter L2C104 attenuates frequencies beyond the upper measurement limit. The filter output is connected through the normally-closed contacts of MONITOR SEND FREQ switch S11 to capacitor C30. When capacitor switch S22 is activated, a sample of the send signal is connected to permit measurement of the send frequency. The output from C30 (VAC) connects to an average/quasi-rms detector. The detector converts the full-wave rectified signal to an average dc voltage.

5.72 The filter output also feeds the auto-ranging and measurement circuits through normally-closed contacts of momentary DAMPING switch S13. When activated, S13 enables the long-time-constant damping circuit U73. This circuit reduces the effects of short-term input signal variations of noise measurements.

5.73 Table 5—1 reviews receive section input power levels, ranges, attenuation, gain, and the measurement window. The table assumes that 600- and 135-ohm signals have been normalized into 900-ohm signals. The dBm equivalents of noise dBrn ranges are shown. The translated level figures are those realized at A4U8 output. The output voltage (VDET) of the detector is proportional to the amplitude of the signal within the measurement window.

5.74 Receiving circuits necessary to establish an appropriate noise impulse peak detection level are on the display driver board. The input amplifier U2 provides 17 dB gain. Step attenuator Q19-Q21 offers 0, 10, or 20 dB attenuation, as set with LOW THRESHOLD control S16D1. This 20-dB range in conjunction with the 60-dB range of the 0-60 dB attenuator, controlled by S1D2, provides an additional 9-dB range. The noise impulse peak at the precision rectifier is thus controllable over an 89-dB range in 1-dB steps. The rectifier converts bipolar inputs to unipolar pulses, sent to the impulse noise measurement section.

Table 5—1. Receive Section Attenuation/Gain Values.

RANGE		LEVEL (DBM)		AUTO RANGE ATTEN (DB)	NOMINAL RECEIVE SECTION GAIN (DB)	TRANSLATED TONE LEVEL (DBM)
R7		+15 to − 2		60	46.8	+1.8 to −15.2
R6		+ 2 to −12		50	46.8	−1.2 to −15.2
R5		− 8 to −22		40	46.8	
R4		−18 to −32		30	46.8	
R3		−28 to −42		20	46.8	
R2		−38 to −52		10	46.8	
R1		−48 to −62		0	46.8	
R0		−58 to −72		0	56.8	−1.2 to −15.2
RANGE	**CIRCUIT NOISE OR NOISE WITH TONE (DBRN)**	**CIRCUIT NOISE OR NOISE WITH TONE (DBM EQUIVALENT)**		**AUTO RANGE ATTEN (DB)**	**NOMINAL RECEIVE SECTION GAIN (DB)**	**TRANSLATED NOISE LEVEL (DBM)**
R7	85 to 68	− 5 to −12		60	66.8	+1.8 to −15.2
R6	72 to 58	−18 to −32		50	66.8	−1.2 to −15.2
R5	62 to 48	−28 to −42		40	66.8	
R4	52 to 38	−38 to −52		30	66.8	
R3	42 to 28	−48 to −62		20	66.8	
R2	32 to 18	−58 to −72		10	66.8	
R1	22 to 8	−68 to −82		0	66.8	
R0	12 to −2	−78 to −92		0	76.8	−1.2 to −15.2
RANGE	**NOISE TO GROUND (DBRN)**	**NOISE TO GROUND (DBM EQUIVALENT)**	**50-DB PAD ATTEN**	**AUTO RANGE ATTEN (DB)**	**NOMINAL RECEIVE SECTION GAIN (DB)**	**TRANSLATED NOISE LEVEL (DBM)**
R7	135 to 118	+45 to +28	50	60	66.8	+1.8 to −15.2
R6	122 to 108	+32 to +18	50	50	66.8	−1.2 to −15.2
R5	112 to 98	+22 to + 8	50	40	66.8	
R4	102 to 88	+12 to − 2	50	30	66.8	
R3	92 to 78	+ 2 to −12	50	20	66.8	
R2	82 to 68	− 8 to −22	50	10	66.8	
R1	72 to 58	−18 to −32	50	0	66.8	
R0	62 to 48	−28 to −42	50	0	76.8	−1.2 to −15.2

5.75 Auto-ranging signals R0, $\overline{R0+R1}$, and $\overline{R2}$-$\overline{R7}$ are produced by counter U17 and changed to a 1-of-8 code by converter U18. After inversion they are applied to the 0-60 dB step attenuator. The binary counter is clocked upward or downward to yield a setting of the 0-60 dB step attenuator that places the VDET voltage within the measurement window.

5.76 Input signals producing VDET voltages in excess of +70 volts (range 7), in excess of +5.0 volts (other ranges), or less than +0.96 volts (any range) can either not be measured (above the maximum in range 7 or below the minimum in range 0) or require a range change. When VDET exceeds the upper limit in range 7 or remains below the lower limit in range 0, the digit display is blanked. When VDET falls outside the measurement window in all other ranges, the binary counter is clocked up or down to return VDET within the measurement window.

5.77 Comparator U6 compares VDET with upper and lower limit voltages. Two outputs are produced. The VDET < VLL signal is high when VDET is less than the lower limit. Unless in range 0, this produces the CHANGE RANGE signal. The ranging control circuit responds by producing a single CHANGE RANGE clock and by momentarily inhibiting the level measurement circuit ($\overline{\text{MEASURE ENABLE}}$). The low VDET >VLL signal conditions U17 to clock downward. The range count decrements to reduce input attenuation by 10 dB. The now-increased VDET voltage is again compared with the limits. Downward clocking of U17 will continue until VDET falls within the measurement window or until R0 is reached. If VDET then remains below the lower limit, CHANGE RANGE will be inhibited and $\overline{\text{UNDERRANGE}}$ blanks the digital display. The $\overline{\text{UNDERRANGE}}$ signal also inhibits the square wave to the frequency measurement circuit (U37A).

5.78 The VDET > VUL signal from the comparator is produced when VDET exceeds the selected upper limit. This signal produces CHANGE RANGE unless R7 is in effect. A high VDET >VLL signal conditions U17 to clock upwards. The ranging control thus causes counter U17 to increment. The count will continue to increment until VDET falls within the measurement window or until range 7 has been reached. If VDET remains above the upper limit in range 7, CHANGE RANGE is inhibited and the digital display is blanked ($\overline{\text{OVERRANGE}}$). The 14-dB measurement window (17 dB in range 7) provides a 2-dB overlap on the 10-dB range boundaries to avoid frequent range changing when the input signal is near a window edge.

5.79 The binary outputs of U17, the 1-of-8 outputs of U18, and inverted signals R0+R1, R6, R7, and R6+R7 select appropriate starting dBm or dBrn counts as a function of measurement range in the measurement circuits.

5.80 RECEIVE SECTION DETAILED DESCRIPTION

5.81 0-60 dB STEP ATTENUATOR (FIGURE 7—22)

5.82 Limiting diodes CR1 and CR2 protect the attenuator against excessive input levels (about +20 dBm in 900 ohms, +22 dBm into 600 ohms, or +28 dBm in 135 ohms). FET switches Q3 through Q9 set the attenuation of stick attenuator R4 through R17 between 0 and 60 dB in the 10-dB steps. The attenuator control includes FET switch drivers Q10-Q16. The drivers convert the logic level ranging control voltages to switching voltages (OFF = 10 V; ON = 0 V).

5.83 GAIN STAGES (FIGURE 7—22)

5.84 Stages U4, U7, and U8 amplify and normalize input signals.

- ☐ The 8.24-dB voltage differential between 135- and 900-ohm circuits for a given input is normalized by U4.
- ☐ The 1.76-dB voltage differential between 600- and 900-ohm circuits for a given input is normalized by U7.
- ☐ A 10-dB increase in gain needed to accomodate the lowest input range (RO) is provided by U8.
- ☐ The 20-dB offset between the tone level input range and equivalent noise ranges is provided by U8.

5.85 Amplifier U4 has a gain of 11.2 dB for 600- 900-ohm operation. This gain is set by R59, R61, and R62. With REC IMPEDANCE switch S7 at 135, the gate of Q31 is grounded to place R60, R142, and R143 in parallel with R59 and R61. The decreased input resistance increases the gain. Calibration potentiometer R143 is set for that 135-ohm circuit gain which yields the specified test set level measurement accuracy.

5.86 The output of U4 is coupled through low-pass filter R279, L1 and C102 and the filter select circuit to U7. The low-pass filter attenuates frequencies above the test set's measurement range. See paragraph 5.90 for a discussion of the filter circuit. Amplifier U7 has a

gain of 18.7 dB when REC IMPEDANCE switch S7 is set at 135 or 900. This gain is set by R103, R104, and R145. When S7 is set at 600, the gate of Q32 is grounded. The FET shunts R145 with R144 and R146 to increase the gain. Calibration potentiometer R146 is set to obtain that 600-ohm circuit gain that yields specified test set power measurement accuracy. The output of U7 connects to U8 and to impulse noise circuits.

5.87 Amplifier U8 has four nominal gain values.

- ☐ 17 dB: Ranges 1-7 in level and frequency measurement modes
- ☐ 27 dB: Range 0 in level and frequency modes
- ☐ 37 dB: Ranges 1-7 in noise measurement modes
- ☐ 47 dB: Range 0 in noise measurement modes

Figure 5—1 shows how feedback and input resistances of U8 are switched to obtain these values. When in level and frequency measurement modes and in range 0, series-connected feedback resistors R106-R108 and parallel-connected resistors R109 and R111 set the gain at 27 dB. When in level or frequency measurement mode and not in range 0, feedback resistors R106-R108 are paralleled by R112 to R113 to reduce the gain by 10 dB. Calibration potentiomenter R113 sets the exact gain required to achieve specified level measurement accuracy. When in noise measurements mode, series-connected resistors R110 and R140 become the input resistance. In range 0, calibration potentiometer R140 is set for a gain of 47 dB to achieve specified noise measurement accuracy. In any range other than zero, series-connected resistors R114 and R115 are connected in parallel with feedback resistors R106-R108. Calibration potentiometer R115 is set for a gain of 37 dB to achieve required noise measurement accuracy in ranges above range 0.

5.88 AUDIO MONITOR (FIGURE 7—22)

5.89 The 0-60 dB step attenuator output range spans 27 dB among ranges R0-R7. To avoid a corresponding and thus bothersome audio monitor output power range, the audio monitor uses compression stages. The output of U1 is coupled to U2A through C8. Amplifier U2A has a gain of 30 dB. The output of U2A drives compression amplifier U2B. Diodes CR49 and CR50 in the feedback path act as non-linear resistances and decrease the gain exponentially as input power increases. The maximum gain of the stage is adjustable by VOLUME control R3. Amplifier U3A operates in the same manner as U2B except feedback current is extracted from the push-pull output pair Q1 and Q2. Diode CR3 minimizes crossover distortion. Figure 7—23 shows connection to the speaker for both test set configurations.

5.90 NOTCH, BANDPASS, AND NOISE FILTERS (FIGURE 7—22)

5.91 To obtain accurate circuit noise measurements on lines conveying a 1004-Hz (or 1000-Hz) holding tone, it is necessary to strip the tone from the noise. When FUNCTION switch S9 is in NOISE WITH TONE position, amplifier U1 and filter U13 are inserted into the signal path. The filter attenuates signals within 15 Hz of 1010Hz by 50 dB. The 6-dB insertion loss of U13 is offset by the 6-dB gain of U1.

5.92 To determine the portion of a tone level measurement attributable to noise, the bandpass filter (U5 and U6; sheet 2 of Figure 7—22) is inserted by pressing momentary BP FILTER switch S12. The bandpass filter range is 200 Hz to 10 kHz. The filter includes four active stages. The first two stages (U5A and B) are

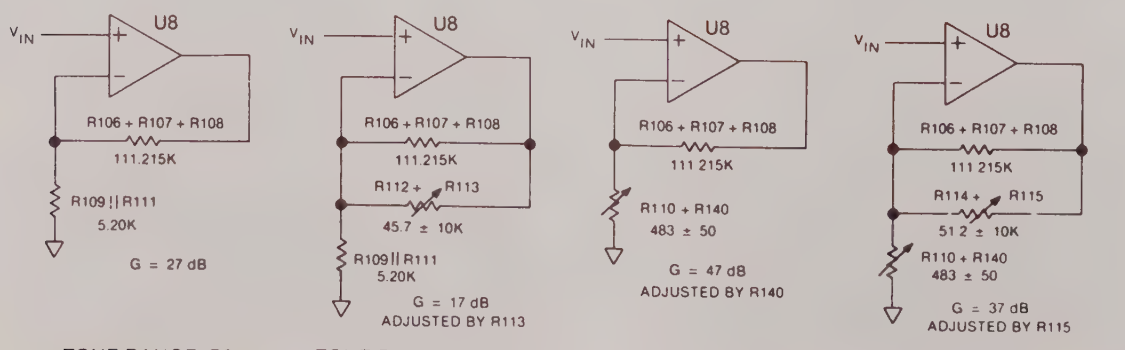


Figure 5—1. Third Gain Stage Configuration.

high-pass filters. The two final stages (U5A and B) are low-pass filters. The insertion loss within the bandpass is set at 0.0 dB with calibration potentiometer R74. Secondary voltages to active the filter are applied to this circuit by S10.

5.93 WEIGHTING switch S10 selects one of five filters, enabled only in a noise position of FUNCTION switch S9D. The characteristics of each filter are presented graphically in Figures 2–1 through 2–5. The 3- and 15-kHz flat filters each include two emitter followers. High frequency roll-off is provided by L networks (R77-C31, R82-C33). Flatness is enhanced by feedback (C30, C32).

5.94 C-MSG filter Q1-Q8 includes a stage of gain (Q1, Q2), a high-pass emitter follower pair (Q3, Q4), a low pass filter and driver (R12, C5, Q5), a low-pass emitter follower pair (Q6, Q7), and a second low-pass filter and drive (R18, C8, Q8). The insertion loss is set at 0.0 dB by poteniometer R5.

5.95 Program filter Q22-Q29 includes a stage of gain (Q22, Q23) and three low-pass emitter follower pairs. The slope on the low-frequency edge of the bandpass characteristic is established by the feedback characteristic in the second and third emitter follower pairs. The insertion loss is set at 0.0 dB by R141.

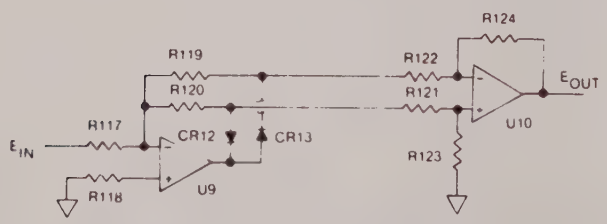
5.96 50kb/s filter A4A2 includes a stage of gain (U1) and low-pass filter L1-L3 and C3-C7. The insertion loss is set at 0.0 dB by GAIN CAL potentiometer R4. Secondary voltages are applied by S10.

5.97 Secondary power is switched to the selected filter by S10. The positive and negative 12-volt supplies are de-coupled by Q33 and Q34, respectively (Sheet 3 of Figure 7–22). Capacitors C65 and C67 provide filtering. The voltage of each transistor output is about 10 volts.

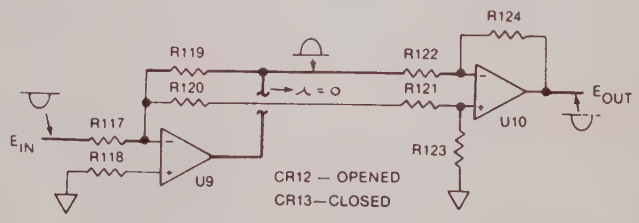
5.98 RECTIFIER-FILTER (FIGURE 7–22)

5.99 This stage includes rectifier U9-U10 and filter U11-U12. Figure 5–2 illustrates rectifier operation. Full-wave rectification is provided by CR12 and CR13, as shown in Figure 5–2A. As shown in Figure 5–2B, negative-going input voltages cause CR13 to close. The gain of U9 in this condition is determined by R119 and R117. The positive-going pulse from U9 produces a negative-going pulse at U10 output. The gain of U10 in this condition is determined by R120 and R117. The negative-going pulse from U9 to the non-inverting input of U10 produces a negaitve pulse at U10 output. Resistors R121 and R123 divide the pulse amplitude by two-thirds. The gain of U10 is determined by R124 and R122, as before. The over all rectifier-filter gain is about 9 dB.

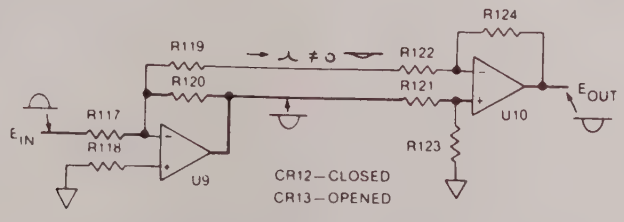
5.100 In the tone level and frequency measurement modes, the filter delivers a voltage proportional to the average value of VAC. In noise measurement mode, the filter delivers a dc voltage related to the rms value of VAC. Figure 5–3 shows the two filter circuit configurations that produce these characteristics. In level and frequency measurement modes, the rectifier output is connected through filter input resistor R128. Capacitor



A — SIMPLIFIED SCHEMATIC



B — EQUIVALENT CIRCUIT FOR NEGATIVE INPUT



C—EQUIVALENT CIRCUIT FOR POSITIVE INPUT

Figure 5–2. Rectifier Circuit.

C57 in the feedback path filters the rectifier output. The gain of the filter is set by calibration potentiometer R129 which is adjusted in level mode in range 0. Offset potentiometer accuracy in the lower regions of the measurement window. Potentiometer R113 is set to achieve accuracy in the upper ranges of the measurement window.

5.101 In noise mode, the rectifier output is applied to noise weighting network D3, D4, R125, and C56. This network delivers the same current to U12 for white noise inputs as for sinusiodal inputs of the same power. The drop across D3 and D4 is compensated by insertion of D1 and D2 in series with R124 in the noise positions of FUNCTION switch S9. Offset potentiometer R133 is set to achieve rated noise power measurement accuracy in the lower regions of the measurement window. Potentiometers R115 (R0) and R140 (R0) set measurement accuracy in the upper regions of the window.

5.102 DAMPING CIRCUIT (FIGURE 7–19)

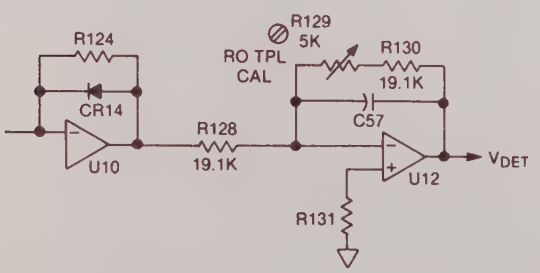
5.103 The rectifier-filter output VDET is connected to logic board A3 via QD45 on A3. This voltage is applied to level measurement comparator U13, frequency measurement circuit buffer U34, and auto-ranging limit comparators U6A and B, all through normally-closed contacts of DAMPING switch S13C. The voltage is also connected to damping circuit U73A through R71 and to R74.

5.104 When S13 is activated, damping circuit U73A is inserted into the circuit by S13C. The long time constant of R71 and C36 suppresses the amplitude of short-term voltage variations on VDET. Amplifier U73A feeds the filtered voltage to S13C. The gain of U73A offsets the loss of divider R70 and R74. (Note that the virtual ground at U73-6 is reflected by diode- connected transistors Q4 and Q5 (part of U74) to R74 via S13A pins 2 and 3.) Portions of the circuit including U73 and U74 are relevant only to a meter circuit, not used in the Model 4002.

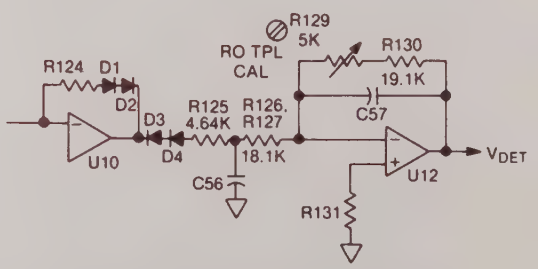
5.105 The damped or undamped VDET voltage is limited at about 7.5 volts by Q9, set by the 8-volt reference voltage, R68, R69, and CR17.

5.106 AUTO-RANGING CIRCUITS (FIGURE 7–19)

5.107 The reference voltages representing the upper and lower limits of the level and noise measurement circuit are provided by U5, Q4, and Q5, shown on sheet 3 of Figure 7–19. Amplifier U5 has a gain of 1.6. The +5-volt input from the precision supply on the analog board thus produces an 8-volt output from U5. This voltage is applied to limiter Q9 (sheet 1) and to two voltage dividers. Divider R19 and R20 supplies the low limit voltage (VLL, +0.96 volts). Resistor R24 is part of the high limit divider. In range 7, the R7 control signal opens switch Q5. When Q5 is open, the gate of Q4 goes negative. Switch Q4 opens and thus removes R25 and R26 from the high limit divider. Resistors R24 and R35 supply +7.0 volts in this condition. When not in range 7, R25 and R26 are in the circuit. The high limit divide nominal output is +5.0 volts in this condition. In practice, this voltage (VUL) will be set to establish the correct span of measurement in ranges 0 through 6. Two voltages are required to represent the upper limit because the span of measurement is 17 dB in range 7 and 14 dB in all other ranges.



A—LEVEL AND FREQUENCY MEASUREMENT MODES



B—NOISE MEASUREMENT MODES

A01998

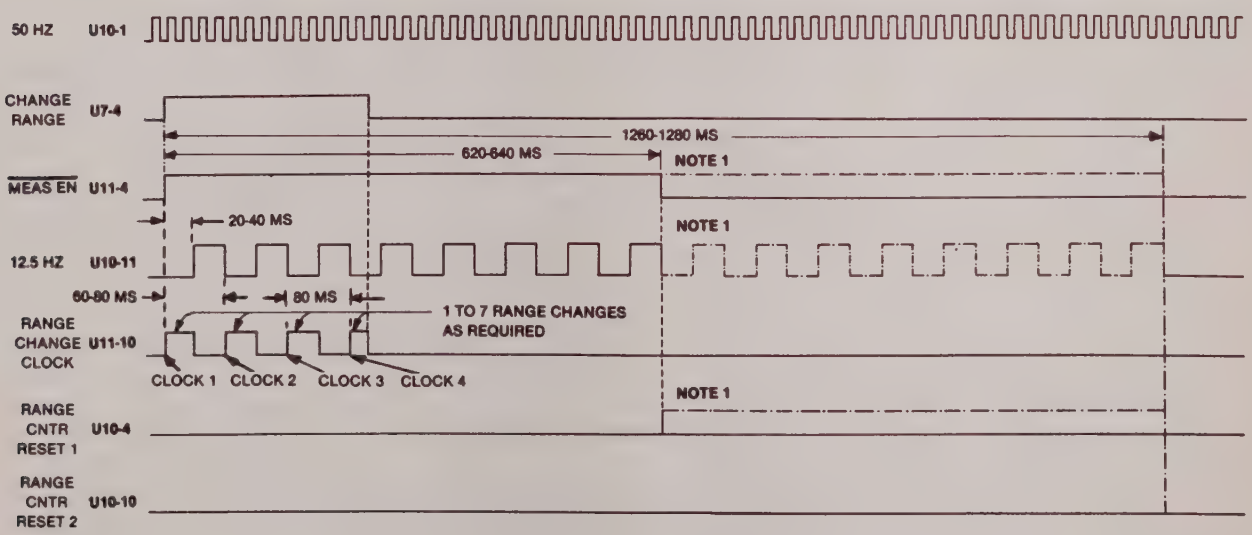
Figure 5—3. Filter Circuit.

5.108 Comparator U6A determines whether VDET is above or below the lower limit. The comparator output at U6-1 (VDET<VLL) is at a logic high level when VDET is above the lower limit (**i.e.**; greater than +0.96 volts). Comparator U6B determines whether VDET is below or above the upper limit. The comparator output at U6-7 (VDET<VUL) is at a logic high level when VDET is below the upper limit. The connection of U6A output to R21 and the connection of U6B output to R23 via Q6 provide hysteresis. When VDET exceeds VLL, U6-1 is at +12 volts. The current through R22 (and R21) from this source displaces the voltage at U6-3 upward from VDET. The amount of displacement is about 1 dB. Thus, U6A will not switch state until VDET has dropped more than about 1 dB below the lower limit. This prevents small input signal fluctuations near the lower limit to cause range switching. The amount of displacement at U6-6 is determined by the conduction of Q6. When not in range 7, the base current of Q6 is sourced by U6-7 via R31 and the R7 signal via R32. When in range 7, the base current is sourced only by U6-7. Thus a lower voltage exists at Q6 collector in ranges 0 through 6 than in range 7, resulting in less hysteresis in ranges 0 through 6 than in range 7. This is appropriate in reference to the wider measurement window in range 7.

5.109 Assume that the range is settled at 5 and that VDET is less than VLL. The discussion that follows explains how the ranging control steps the range down until VDET lies between the limits. The low at U6-1 conditions U17-10 so that U17 is clock downward. The output at U7-11 will be high because R0 is low. This causes U7-3 to go low. With DAMPING switch S13 not activated, U7-6 will be low. CHANGE OF RANGE (U7-4) goes high to condition U11-8 and to set latch U11A and B. The low at U11-3 releases reset from U10. The high from U11-4 inhibits the level measurement circuit. Binary counter U10 now delivers a 12.5-Hz clock to U17 via conditioned gate U11C. Each clock decrements the count of U17. The next lowest range is decoded by U18. Inverted outputs of the decoder are connected to the drivers of the 0-60 dB step attenuator and A4U8 via logic on logic board B. As the ranging steps downward, VDET rises. The ranging is stepped downward at a 12.5 steps per second until VDET exceeds VLL (or until R0 is reached).

5.110 Binary counter U17 is conditioned to clock upward when VDET exceeds VLL. When VDET exceeds VUL in any range except 7, U7-10 goes high. The output of U7-4 conditions U11-8 and sets latch U11A and B as described in paragraph 4.109. The contents of U17 are now clocked upward. The range is stepped until VDET falls below VUL or until range 7 is reached.

5.111 Counter U10 clocks to count 32 each time the latch is set. The count of 32 resets the latch. The interval over which the latch is set (620 to 640 msec) is sufficient to allow the auto-ranging search to be completed before releasing the level measurement circuit; eight 12.5-Hz clocks are included within this interval. Figure 5—4 shows the timing of the circuit.



NOTE 1. QD 23 NORMALLY CONNECTED TO QD 25. DASH-DOT WAVEFORMS OCCUR IF QD 24 IS CONNECTED TO QD 25.

Figure 5—4. Range Change Clock And Measure Enable Timing Diagram.

5.112 When the range steps to R0 and VDET remains below VLL, U9B is conditioned to produce $\overline{\text{UNDER-RANGE}}$. This function inhibits the crossover detector output (paragraph 5.114) and controls display blanking. When the range steps to R7 and VDET remains above VUL, U9C is conditioned to produce $\overline{\text{OVERRANGE}}$. This function controls display blanking.

5.113 The logic for selecting auto-ranging signals R0, $\overline{\text{R0}+\text{R1}}$, and $\overline{\text{R2}}$ through $\overline{\text{R7}}$ or manually-selected noise impulse ranging signals $\overline{\text{R1}}$ through $\overline{\text{R7}}$ is shown in Figure 7–30. Gates U12 and U14 select inputs A in impulse noise mode, inputs B in other modes. Note that R0 is fixed in impulse noise mode. Gate outputs are connected to the analog board via A7J2 and A4J1.

5.114 SINE WAVE-TO-SQUARE WAVE CONVERTER

5.115 CONVERTER U35 and U36 and latch U37B/C provide a square wave with a duty cycle that varies little from 50% with input level and with good (10 dB or better) noise immunity. The zero crossover region of VAC is detected with a threshold that varies with the amplitude of VAC. The threshold voltages at comparator inputs U35-2 and U36-3 are derived from VDET, buffered by U34. The VAC input rides a voltage midway between the thresholds. Figure 5–5 shows the operation of this circuit. The diagram shows threshold voltages 0.27 VDET and 0.11 VDET in relation to VAC, riding 0.91 VDET. Comparator U36 supplies a positive output when offset VAC is negative in respect to 0.00 VDET and a negative output when offset VAC becomes positive in respect to 0.11 VDET. Similarly, comparator U35 output is positive when offset VAC is positive in respect to 0.27 VDET and negative when offset VAC is negative in respect to 0.27 VDET. The latch switches states on the positive-going edges of U35 and U36 outputs. The diagram identifies the region in which the latch is immune to voltage reversals caused by noise.

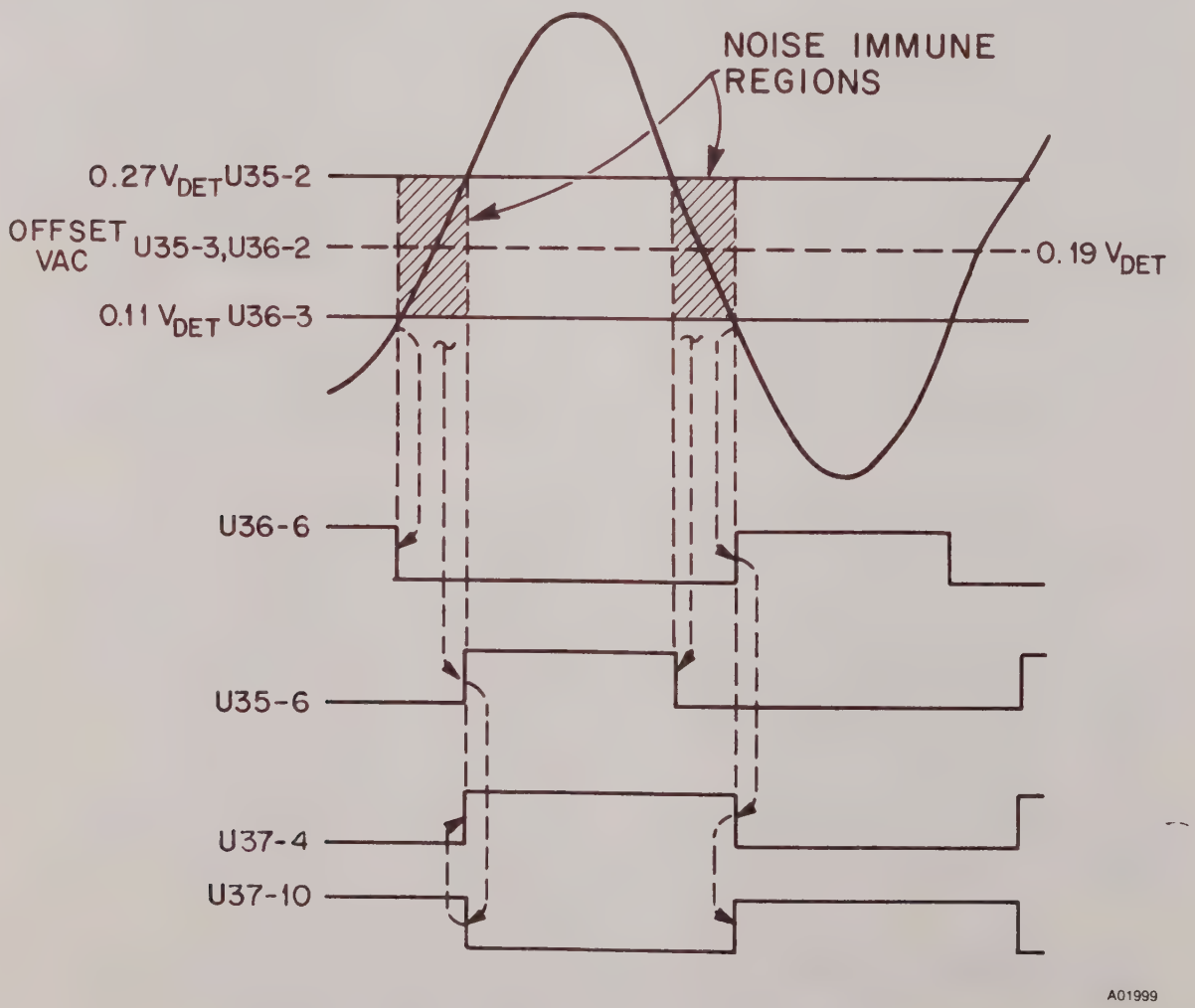


Figure 5–5. Sine Wave-To-Square Wave Converter Waveforms.

5.116 Gate U37A inhibits the latch output (and thus frequency measurement) in the presence of an underrange condition. The $\overline{\text{UNDERRANGE}}$ function is generated by the auto-ranging circuit when the input signal remains below the lower limit of the measurement range in range 0.

5.117 IMPULSE NOISE CIRCUIT (FIGURE 7–32)

5.118 The output of amplifier A4U7 is connected to impulse noise circuits on the display driver board via QD28 on A4 and QD6 on A8. Input amplifier U2 provides 6 to 17 dB gain. LOW THRESHOLD CALIBIRATE potentiometer R39 is set to achieve accurate counts at the lowest of three counter thresholds. The output of U2 passes through 0-20 dB 10 dB step attenuator R40-R44. The attenuation is selected by the decade portion of LOW THRESHOLD switch S16D1 via switch pairs Q19-Q24 (0 dB), Q20-Q23 (10 dB), and Q21-Q22 (20 dB).

5.119 The LOW THRESHOLD (TEN'S) thumbwheel switch S16D1 controls attenuator switches Q19-Q20 and the 0-60 dB step attenuator on the analog board.

5.120 Diodes CR8-10 or the 10-, 20-, and 30-dBrn control functions to produce $\overline{\text{MAN R1}}$, which selects the 0 dB setting of the 0-60 dB attenuator. The manual ranging controls are gated on logic board B. The unit LOW THRESHOLD thumbwheel switch S16D2 controls the gain of amplifier U3. The gain ranges from 40 dB (0 dBrn positions of S16D2) to 31 dB (9 dBrn position) in 1 dB steps.

5.121 The precision rectifier converts the bipolar input to a unipolar (positive-polarity) output. Amplifier U4 and diodes CR11/12 make up a half-wave rectifier. On positive half cycles of the input, the output is clamped by CR11 to the voltage at U4-2. On negative half cycles of the input, diode CR12 closes to enable feedback current through R72. The output through CR12 combined with U3 output, which is connected through R68 and R71. The signals combine such that the positive outputs of U4 convert the negative half cycle of the input to a positive half cycle at the output. The current from U4 in this half cycle is the opposite polarity and double the magnitude of the input current through R68 and R71. The rectifier is out of the circuit during the positive half cycle of the input. Calibration potentiometer R68 equalizes the output amplitude for negative and positive inputs. Potentiometer R95 establishes the quiescent output voltage. This adjustment primarily affects low threshold detection accuracy.

5.122 FREQUENCY MEASUREMENT FUNCTIONAL DIAGRAM (FIGURE 7–5)

5.123 The signal input frequency is counted indirectly. A phase-locked loop tracks the signal frequency, producing an output frequency four times that of the input. The loop includes the 80-Hz to 240-kHz VCO, frequency divider U33, and the phase comparator. The overall frequency range of the VCO is divided into 16 smaller ranges set by the 16 combinations of external capacitance. The error limit detector and the binary counter select the most appropriate range.

5.124 The VCO is enabled by the frequency mode control signal. The VCO output is divided by U33 and then compared with the input signal frequency. The polarity of the resulting error voltage is determined by direction of the difference frequency; the amplitude is determined by the magnitude of the difference in frequency. An error voltage falling between high and low limit voltages is within the selected VCO range. In this condition, counter U30 will not be clocked. The VCO frequency is adjusted by the error voltage to reduce the error to zero. When the error voltage falls outside the limit voltages, counter U30 will be clocked up or down as appropriate. The binary output of U30 changes the combination of capacitances. The count is altered until the error voltage is within limits or until an out-of-range condition is detected.

5.125 When the content of U30 equals 0 and the error voltage remains above the high limit, gate U29D presets counter U30 at 0. This condition persists as long as the error voltage remains above the high limit. The output of U29D signals this condition to the display section as PPL OR.

5.126 Measurement of VCO frequency is accomplished as follows:

- ☐ Starting number 00000 is stuffed into the five-stage counter.
- ☐ The VCO is gated as counter clock for 250 milliseconds.
- ☐ The count accumulated at the end of the 250-millisecond measurement interval is stored.
- ☐ The counter is tested for overflow with each measurement; range is switched as required.
- ☐ Starting number 00000 is stuffed and the sequence repeats.

Frequency gate generator U55, enabled in frequency mode, produces FREQ GATE and the FREQ EOM pulse. The store and stuff control U52 supplies XFR and PE pulses in that order. The PE pulse enables the parallel enter mode of each counter. In frequency mode, the parallel input data to each stage is always zero. Thus, PE has the effect of clearing the counter.

5.127 The 250-millisecond gating interval translates VCO frequency to input frequency. The gated VCO output clocks each counter stage. Stages U38-U42 are designated as digits A-E from highest to lowest order. Count accumulation is enabled in any stage receiving $\overline{co}$ from the next lower stage. Counts accumulate 00000 through 9999 in the Hz range. Stages A-E can accumulate 10.000 kHz through the upper measurement limit in the KHZ range.

5.128 The automatic ranging control on logic board B tests the CARRY outputs from stages A and B. The carry out (co_1) from stage A is tested in the HZ range. This carry out signal signifies 9999 Hz. If less than 9999 counter clocks appear within the current freq gate, the condition for selecting the KHZ range is not established. When the 9999th clock does appear, the circuit detects the condition for the kHz range. The PE signal appearing at the end of the measurement interval sets the kHz mode in this situation. When in the kHz mode, the carry out (co_2) from stage B is tested. This carry out signal signifies a count accumulation of 9.999 kHz. With less than 9999 counter clocks, the range reverts to HZ. With 9999 or more counter clocks, the KHZ range is retained.

5.129 At the end of FREQ GATE, the FREQ EOM pulse to U60 porduces XFR. Stored BCD date is selected sequentially at a rate asynchronous to measurement. The PE signal to the automatic range control assures that range switching occurs only between measurement intervals. A PE pulse follows the XFR pulse to begin another frequency measurement.

5.130 FREQUENCY MEASUREMENT DETAILED DESCRIPTION

5.131 PHASE LOCKED LOOP AND 4X MULTIPLIER (FIGURE 7—19)

5.132 The test set uses a phase locked loop and 4X frequency multiplier during frequency measurements. A simple phase locked loop is an electronic servo loop consisting of a phase detector, a lowpass filter, and a voltage controlled oscillator (vco). The phase detector compares the input frequency with a frequency derived from the vco and produces an error signal proportional to the phase difference. The error signal, averaged into a control voltage by the loop filter, pulls the vco frequency to bring the error signal to zero. The phase locked loop used in this test set has several additional components to enhance the range and increase the speed.

5.133 The divide-by-four circuit reduces the vco frequency so that the phase detector input frequencies have a 1:1 ratio. This lets the vco operate at four times the input frequency for faster display updates without loss of accuracy. The limit comparator and up/down control, range selector counter, and range capacitor selector make up a form of autoranging to control the vco with 12% to 88% range of the control voltage. The circuits also add capacitance to give the vco an 80-Hz to 240-kHz frequency range.

5.134 PHASE DETECTOR AND LOOP FILTER (FIGURE 7—10)

5.135 The phase detector (p/o of U32) produces a pulse with proportional to the phase difference between Fin and 1/4 Fvco. A "1" is produced if Fin > 1/4 Fvco and a "0" if Fin < 1/4 Fvco. The phase detector presents a high output impedance when Fin = 1/4 Fvco. The error signal consisting of "1" and "0" goes to the loop filter circuit.

5.136 The loop filter includes a slow response filter (R46, R47, C25, C26) for high noise immunity and a fast response filter (R48, C26, CR12, CR13) to increase the slewing rate. Under near lock conditions (Fin ~ 1/4 Fvco) the phase detector provides very narrow pulses. In this case, the long time constant of the slow filter produces a slow control voltage output not susceptible to noise. If Fin ≠ 1/4 Fvco, diodes CR12 and CR13 conduct through resistors R48 allowing the control voltage to change much more rapidly. The control voltage drives the vco as well as the limit comparator and up/down control.

5.137 VOLTAGE CONTROLLED OSCILLATOR (FIGURE 7—19)

5.138 The vco is part of U32. The vco is a wide-range CMOS oscillator. Frequency is determined by: (a) external resistance and capacitance and (b) the control voltage. The output of the vco is a square wave that swings between 0 and +12 volts. A high F (frequency measurement mode) enables the vco via transistor switch Q8. Thus, the phase locked loop operates only during a frequency measurement.

5.139 The vco operates with a control voltage between 12% to 88% of the operating voltage (12 Vdc). However, use of a single resistance-capacitance combination would not allow the vco to have an 80 Hz to 240 kHz range while operating with the 12% to 88% control

voltage. Switched combinations of external capacitors permit 16 ranges within the 80 Hz to 240-kHz overall range.

5.140 LIMIT COMPARATOR, RANGE SELECTOR COUNTER, AND RANGE CAPACITOR SELECTOR (FIGURE 7–19)

5.141 Voltage divider R38/R39/R40 applies the 12% and 88% points of the operating voltage as thresholds to comparators U28A and U28B. A control voltage less than the low threshold causes the output of comparator U28A to go high while comparator U28B output remains low. This results in a "1" on the output of inverter U29B and a "0" on the output of nor-gate U29A. The resulting "10" code instructs range selector counter U30 to increment at a 100-Hz rate until the control voltage rises above the 12% threshold point. Likewise, a control voltage above the 88% threshold point produces a "00" code. This code commands the selector counter to decrement until the control voltage falls below the 88% threshold point. The four-bit binary output of the counter operates the range capacitor selection.

5.142 If, when attempting to reduce the control voltage below the 88% threshold point, the counter is required to decrement past zero then gate U29 freezes the counter in the "0000" state. The gate also applies a high PLL OR (phase locked loop overrange) to the display blanking and polarity circuit as long as the countdown condition persists. An "11" code indicates that the control voltage falls within the optimum range and holds the counter in its present state. The 4-bit binary output of the counter operates the range capacitor selector.

5.143 The range capacitor selector consists of four transmission gates (U31), a bank of four capacitors (C14-C17), and one capacitor (C9) always connected to the vco. Up to sixteen capacitance values can be added to the vco by the 4-bit binary input. Only capacitor C19 remains connected to the VCO with a "0000" (least capacitance) 4-bit binary input. A "1111" 4-bit binary input adds all four capacitor (C14-C17) to vco. Adding capacitance to the vco reduces its maximum frequency of oscillation.

5.144 250-MILLISECOND TIMER (FIGURE 7–19)

5.145 The 250-millisecond time generates a 250-millisecond FREQ GATE every 260 milliseconds. During the FREQ GATE positive interval, PLL DATA is gated to clock the data counter. The timer, in conjunction with the data transfer (store) and counter stuffing circuit, also generates the FREQ EOM control signal.

5.146 The timer consists of ring counter U55A/U55B/U54A, flip-flops U60A and U60B, and latch U57C/U57D. The timer, when enabled by a low F (frequency measurement), uses a very accurate 100-Hz clock to generate the 250-millisecond FREQ GATE. Figure 5–6 shows the various waveforms generated by the timer.

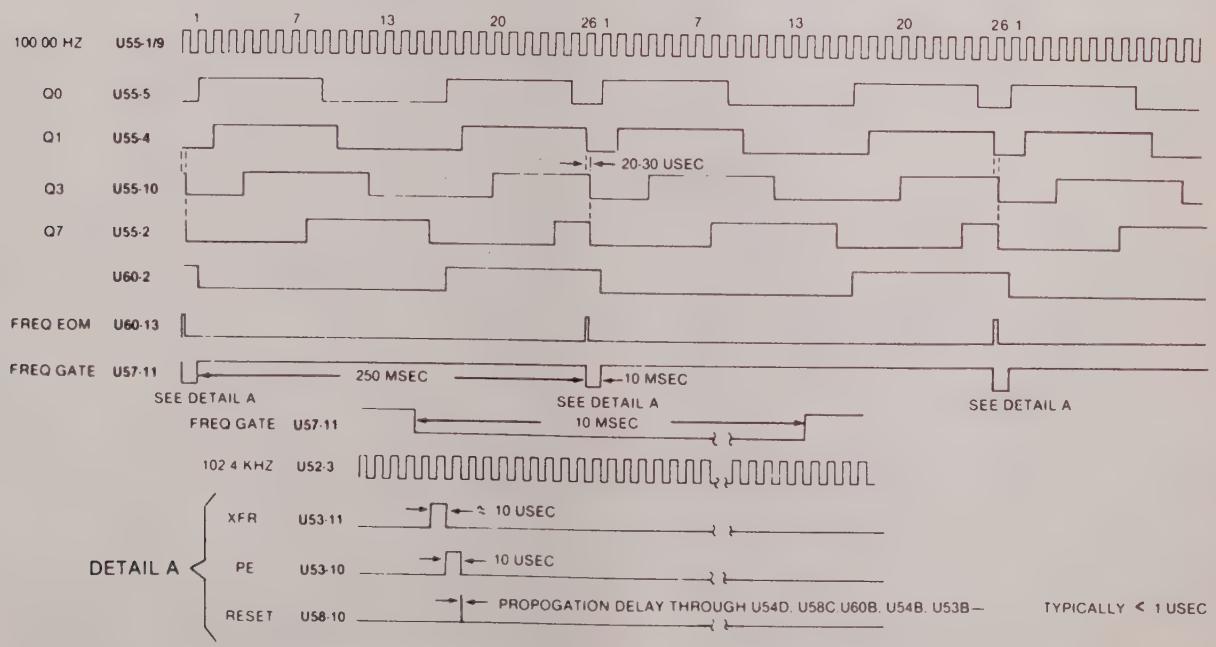


Figure 5–6. Millisecond Timer Waveform Diagram.

5.147 DATA COUNTER (FIGURE 7–19)

5.148 Each counter stage U38-U42 has five inputs.

- ☐ The PE input enables parallel entry via P1-4.
- ☐ The parallel BCD input represents a starting number to be stuffed (00000 in frequency mode).
- ☐ The clock represents events to be counted (cycles of the input signal in frequency mode).
- ☐ An input to the UP/DN control (always UP in frequency mode).
- ☐ A carry out ($\overline{co}$) from the next lower stage enables accumulation of count stage E is always enabled.

Each counter has two outputs.

- ☐ The carry out ($\overline{co}$) output signifies that the stage is holding a count of 9.
- ☐ The BCD output of each stage represents a decimal digit and is made available to registers U44-U47 for storage or, in the case of digit E, to quick-disconnect pins 14-17 for readout during test set calibration.

The carry out form digit E to digit D is controlled in frequency mode and in kHz range, gate U43B configures the counter into a five-stage counter.

5.149 STORE AND STUFF (FIGURE 7–19)

5.150 This circuit includes U52, U53B, U54B, U54D, U58B, and U58C. The inputs include FREQ EOM and the 102.4 KHZ clock. When the frequency gate generator produces FREQ EOM, reset is released from U52 and U53 is enabled. The circuit produces XFR, PE, and RESET as shown in detail A of Figure 5–7A. The RESET pulse terminates FREQ EOM and clears the frequency gate generator. (Gate U54C, gate U58D, and flip-flop U61A are not used in the Model 4002.)

5.151 Frequency Auto-Ranging (Figure 7–32)

5.152 The frequency auto-ranging circuit monitors the carry out $\overline{co_1}$ and $\overline{co_2}$ outputs of the data counter stages A and B to produce the range control signal. When the frequency is less than 9999 Hz, the KHZ/HZ control signal selects digit C decimal point and inserts counter stage E. In the quiescent state, PE clears U5A and U5B to produce a low KHZ/HZ signal. With U5-13 low, U8-5 is conditioned. In this state $\overline{co_1}$ (counter holding 9999 Hz) conditions U8-6 to set U5A. The next STUFF signal sets U5B to produce a high KHZ/HZ signal. In this condition, U5-13 conditions U8-6. This allows $\overline{co_2}$ (counter holding 9.99 kHz or more) to condition U8-5 and thus maintain the KHZ range. Failure of $\overline{co_1}$ to appear while in HZ range will cause the counter circuit to remain in Hz range. Failure of $\overline{co_2}$ to appear in the KHZ range causes the counter circuit to return in the Hz range. The PLL DATA input prevents false circuit operation that might occur during data counter clocking.

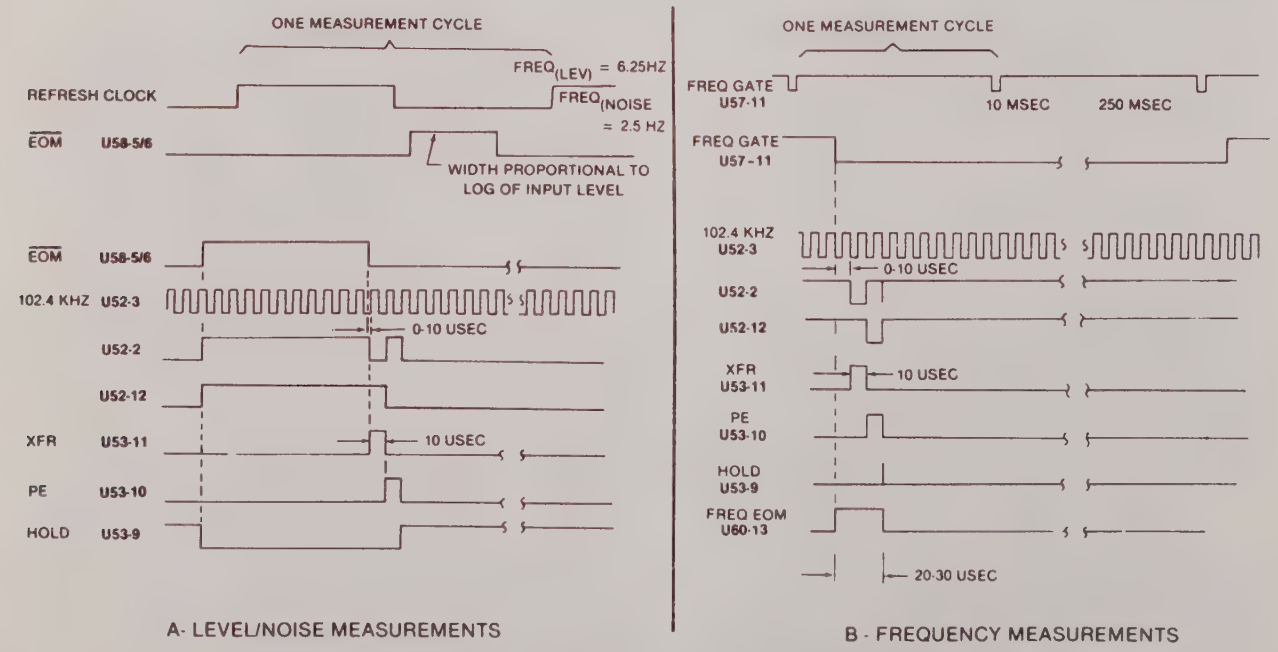


Figure 5–7. Data Transfer (XFR) and Counter Updata (PE) Timing.

5.153 TONE LEVEL MEASUREMENT FUNCTIONAL DIAGRAM (FIGURE 7-6)

5.154 The dc voltage VDET is a logarithmic function of the input signal level at the 0-60 dB step attenuator output. The span is 14 dB in ranges 0 through 6, 17 dB in range 7. To measure the level point within this range, it is necessary to compare VDET with a logarithnic reference. The comparison is made in reference to the maximum level permitted in the range (the same upper limit voltage used in the receive section auto-ranging circuit). The measurement, in terms of dB, is thus downward. The result in dBm is the sum of the maximum input level permitted in the selected range and the measured number of dB. For example, the maximum input level in range 3 is −28 dBm. If the input level is −35 dBm, the level measurement will be −7 dB. To obtain a display of −35 dBm, the counter adds 7 dB to the count and affixes a negative sign. The measurement is made 375 times per minute (6.25 times per second).

5.155 Comparators U13 and U14 compare a periodic, logarithmically decaying voltage with VDET and VUL. The logarithmic reference is supplied by waveshape generator Q3, C10, and R12. These three voltages are shown graphically in Figure 7−6. The function $\overline{VUL > VLOG > VDET}$ defines the interval in which the logarithmic reference decays from the upper limit to VDET. The width of this function increases as the input power decreases within the given receive range. The $\overline{VUL > VLOG > VDET}$ function is enabled when the auto-ranging circuit is settled (at U12B). Also, the function is gated by U15B in synchronism with Q3 control to avoid spurious outputs during flyback of the logarithmic reference. The counter clock is produced by gating the 102.4 kHz clock with $\overline{VUL > VLOG > VDET}$. The number of clocks gated is determined by the width of $\overline{VUL > VLOG > VDET}$, which is a function of the number of dB by which the step attenuator output differs from the maximum permitted. Each clock pulse represents 0.01 dB; the logarithmic reference is calibrated by R13 to decay by an amount representing 0.01 dB per clock period (9.77 microsecond).

5.156 Each measurement cycle starts with the PE pulse. The stuffed number for each range is shown in the table in Figure 7−6. Note that the stuffed number agrees closely with the input level upper limit in each range. Digit E counter is stuffed with 5 so that digit E will be correct to the nearest 0.05 dB. As an illustration, assume that the number 058.00 was stuffed and the measurement yielded five 0.01 dB pulses (U16B output). The counter would hold 058.05 and the display would show 058.0. The display would obviously not be correct to the nearest 0.1 dB. By stuffing 5 into the digit E counter, the display would read 058.1 in this case. To maintain this characteristic in ranges 6 and 7 where it is possible to cross 0.0 dBm, slightly different numbers are stuffed after crossover is detected.

5.157 The five-stage counter counts upward in ranges 0 through 5. Gates U15C, U26A, and U26B control the count direction in level measurement mode. The counter can count downward only in range 6 and range 7, and then only if crossover has not been detected. Assume that the input power is −3 dBm and that auto-ranging has settled in range 6. At the start of the measurement cycle, the number 002.05 is stuffed. Measurement begins and U16B delivers clocks to the counter. The counter clocks downward. When the count moves from 00001 to 00000, each counter stage produces a carry out signal. The product of the carrier ($\overline{00000}$) sets crossover latch U15. The $\overline{co}$ output causes U26B output to change state. Measurement continues but the counter clocks upward until reaching the number 002.95. The display will read −2.9 dBm. The crossover latch remains set while the ensuing XFR and PE pulses are produced. The new starting number 001.95 is stuffed. The crossover latch is reset only after stuffing is complete. Another measurement is made exactly as before. However, the result with the corrected starting number is 003.05 and −3.0 dBm is displayed.

5.158 The PE pulse clocks U61B and thus samples LEV 0 dBm. When a range 6 or range 7 measurement has been completed without having detected crossover, U61B is set to activate the vertical segment of the polarity indicator. (The horizontal segement is activated by the level measurement signal.)

5.159 Storage of results and subsequent collection of data by the display circuits in the level measurement mode do not differ from the frequency measurement mode.

5.160 **TONE LEVEL MEASUREMENT DETAILED DESCRIPTION (FIGURE 7−19)**

5.161 The tone level measurement sequence is similar to that in the frequency measurement mode.

- ☐ A starting number is stuffed into the counter.
- ☐ The receiver analog output is converted to a digital representation of dB down from the upper window edge.

This is combined with the stuffed number in the counter.

- ☐ A test for 0.0 dBm crossover is made during measurement.

- ☐ The accumulated count is stored and the crossover test result is sampled.
- ☐ A starting number is stuffed. In range 6 or 7 this number depends on the crossover test result. This sequence repeats 375 times per second.

5.162 STUFFING LOGIC

5.163 Stuffing logic is shown of Sheet 3 of Figure 7—19. Five BCD output sections, one per digit, are shown. The output numbers in level measurement are listed in Figure 7—6.

- ☐ Digit A in always 0 in level measurement mode.
- ☐ Digit B is gated by the lower four AND gates of U21 and formulated by U22 and U23, which are conditioned by auto-ranging signals.
- ☐ Digit C is generated by U19D, U23B, U24, U25, and U26C.
- ☐ Digit D is either 0 or 9 in level measurement mode, as determined by U26C, U8B, and U25C.
- ☐ Digit E is always 5 in level measurement mode.

5.164 ANALOG-TO-DIGITAL CONVERTER

5.165 The analog-to-digital converter is shown on Sheet 1 of Figure 7—19. The converter includes gated logarithmic reference generator Q3, comparators U13 and U14, and output gating. In level measurement mode, Q3 is gated by the 6.25 Hz square wave. When Q3 is OFF, C10 charges rapidly to +7.2 volts through CR1 and R11. When Q3 is ON, CR1 opens and C10 discharges through R12 and calibration potentiometer R13. The voltage from full discharge to termination of the measurement represents a span of at least 17 dB in terms of VDET range. Potentiometer R13 is set during calibration to optimize measurement accuracy within the 10-dB range mid-way between the extremes of the 14-dB measurement span.

5.166 The logarithmic reference VLOG is compared with VDET and VUL by U13 and U14. The upper limit voltage is the same as that used in the auto-ranging circuit as the upper limit (7.0 volts in range 7; +5.0 volts in ranges 0 through 6). The relationships among VDET, VLOG, and VUL are shown in Figure 5—8. The outputs of U13 and U14 ($V_{LOG} > V_{DET}$ and $V_{UL} > V_{LOG}$) are AND-ed by U9A to produce $\overline{V_{UL} > V_{LOG} > V_{DET}}$. This pulse has a width that varies directly with the amount by which VDET lies below the upper

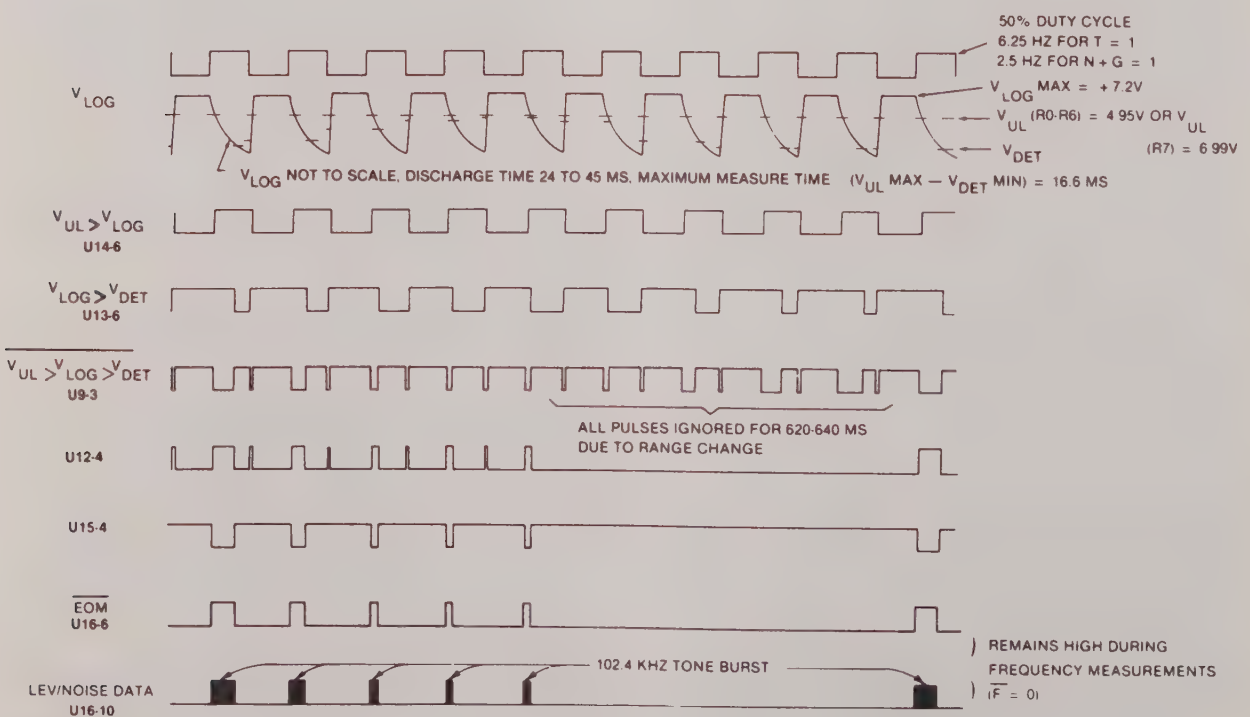

50% DUTY CYCLE
6.25 HZ FOR T = 1
2.5 HZ FOR N + G = 1
VLOG
VLOG MAX = +7.2V
VUL (R0-R6) = 4.95V OR VUL (R7) = 6.99V
VDET
VLOG NOT TO SCALE. DISCHARGE TIME 24 TO 45 MS. MAXIMUM MEASURE TIME (VUL MAX — VDET MIN) = 16.6 MS
VUL > VLOG U14-6
VLOG > VDET U13-6
VUL > VLOG > VDET U9-3
ALL PULSES IGNORED FOR 620-640 MS DUE TO RANGE CHANGE
U12-4
U15-4
EOM U16-6
REMAINS HIGH DURING FREQUENCY MEASUREMENTS (F = 0)
102.4 KHZ TONE BURST
LEV/NOISE DATA U16-10

Figure 5—8. Level/Noise Logger Timing Diagram.

limit. The width is 9.77 microseconds per 0.01 dB. Gate U12B inhibits this pulse when auto-ranging is not settled. Gate U15B masks spurious pulses produced during the charge cycle of C10. Gate U16A inhibits the pulse in frequency measurement mode. Gate U16B enables 102.4 kHz pulses through the pulse interval. Note that the period of the 102.4 kHz clock is 9.77 microseconds. Because of scale factor of the pulse from the comparator is 0.01 dB per 9.77 microseconds, each clock represents 0.01 dB.

5.167 Store and Stuff Circuit

5.168 The EOM pulse controls stuff and store circuit U52 and U53 through U58B and U54B. The operation of this circuit in level measurement mode does not differ from that in frequency measurement mode. The circuit becomes active immediately following the negative-going transition of EOM. See Figure 5–7A. The frequency gate generator is not enabled in level measurement mode.

5.169 Counter and Crossover Circuits

5.170 The gated 102.4 kHz clock is coupled by U57A to the clock inputs of counter stages A-E. The counter is clocked upward or downward in accordance with the states of U15C inputs. The count is always upward in ranges 0-5 (R6 and R7 will be low at U15-9). the count commences in the downward direction in ranges 6 and 7 (both inputs are high at U15C to begin a measurement). The zero crossover signal ($\overline{co}$) goes low to reverse count direction only when the counter content decrements from 00001 to 00000 Gates U56A, U56B, and U56C AND the carry out outputs of the counter. The product sets crossover latch U15A/U15D. The normal latch state is low at U15-3 and high at U15-11, reversed when crossover is detected. At this time, $\overline{co}$ goes low to switch the counter up/down control to high state. The crossover latch is reset between measurements by the 6.25-Hz REFRESH CLOCK.

5.171 The outputs of the crossover latch affect stuffing of digits C and D. Note that the STUFF pulse appears before the latch is reset.

5.172 NOISE MEASUREMENT FUNCTIONAL DIAGRAM (FIGURE 7–7)

5.173 The dc voltage VDET characteristics in noise measurement modes are similar to those in level measurement mode. The voltage is a logarithmic representation of equivalent noise power of the 0-60 dB step attenuator output and has the same spans (14 and 17 dB). Analog-to-digital conversion differs only in that 150 measurements per minute are made.

5.174 Stuffed numbers are shown in a table in Figure 7–7. As in level measurement mode, the numbers relate to the signal input upper level limit of each range. The $\overline{CN + NWT + NTG}$ control function allows count accumulation only in the downward direction. Note that digit B is stuffed with a number exceeding the range number by 1 in the count noise and noise with tone modes and with a number exceeding the range number by 6 in noise to ground mode (with carry unit number by 6 in noise to ground mode (with carry appearing in digit A). Digit C is always stuffed with the unit digit given in the figure for the upper level limit in the selected range.

5.175 In range 0, the measurement window actually extends to –2 dBrn. It is necessary to blank results less than 0 dBrn. Crossover latch U15 detects the counter transition from 00001 to 00000 and sets 0 dBrn latch U62 when this occurs. The output of gate U62B blanks the display and activates the horizontal (minus) segment of the polarity indicator. The crossover latch is reset between measurements. The 0 dBrn latch is reset by the PE pulse.

5.176 NOISE MEASUREMENT DETAILED DESCRIPTION (FIGURE 7–19)

5.177 The noise measurement sequence is similar to that in the level measurement mode.

- ☐ A starting number is stuffed into the counter.
- ☐ The receiver analog output is converted to a digital representation of dB down from the upper window edge. This is combined with the stuffed number in the counter.
- ☐ A test for 0.0 dBrn crossover is made during measurement.
- ☐ The accumulated count is stored for subsequent display (unless noise is less than 0.0 dBrn).
- ☐ A starting number is stuffed. This sequence repeats 150 times per minute.

5.178 The stuffing numbers are set up as follows:

- ☐ Digit A is set at 1 in ranges 4-7.
- ☐ Digit B is set at the range number plus 1 in circuit noise and noise with tone modes or at the range number plus 6 in the noise to ground mode by U8E, U19A, U19B, and U20.
- ☐ Digit C is set at 2 or 5 by U19D, U24C, and U24D.

☐ Digit D is set at 5.

☐ Digit E is set at 0.

5.179 The 2.5 Hz square wave is selected as REFRESH CLOCK by U12D (Sheet 1 of Figure 7—19). Crossover latch U15 is set by U59-4 when crossover occurs. The 0-dBrn latch U62 is set by U15-3 at that time. The output of U62-4 blanks the digital display and activates the minus segment of the polarity indicator.

5.180 IMPULSE NOISE MEASUREMENT FUNCTIONAL DIAGRAM (FIGURE 7—8)

5.181 The unipolar pulse from precision recitifier A8U4 on the display driver board has a peak voltage representing test set input peak level. The lowest countable rectifier output represents an input pulse having the peak level given by the settings of the LOW THRESHOLD thumbwheel switches. The rectifier output range extends upward from that point at least 12 dB.

5.182 Three comparators detect pulses at the LOW THRESHOLD and two higher levels separated by 2, 4, or 6 dB. The threshold circuit for comparators U5-U7 include a precision voltage divider, THRESHOLD SEPARATION thumbwheel switch S16D3, and switches Q25-Q30. The comparator outputs trigger counters on logic board A.

5.183 Three identical, independent, four-stage BCD counters accumulate records of LO LEVEL, MED LEVEL, and HIGH LEVEL events. Each counter is clocked through a 140-msec blanker, which masks the counter from the associated comparator for 140 milliseconds after each detected pulse. Each 140-msec blanker thus limits the count rate at about 7 pulses per second. The clock from each 140-msec blanker enabled only when the content of the associated counter remains below 9999 and when TIME OUT is not active. The counters are disabled when not in impulse noise mode ($\overline{\text{ENABLE}}$). When activating the impulse noise mode, the delayed release circuit holds the counters off for 160 millisecond to avoid counting of spurious receiver outputs caused by switching.

5.184 The four stages of each counter are designated A-D, from highest to lowest order. The outputs interface with the display section.

5.185 Timed collection of data is implemented by counters U10 and U20, preset to the desired interval with thumbwheel switches S16D4 and S16D5. The range is 1 to 99 minutes. A one-minute clock is generated by the divide-by-6000 circuit. The one-minute clock decrements the contents of U10 and U20. Time left is displayed on digits C and D of the display. When the decrementing count changes from 01 to 00, the time out detector produces TIME OUT. This signal inhibits the one-minute clock and defeats the clock gate of each event counter. Event counter contents are retained for subsequent read-out. To reload the time-left counter and reset the event counters, it is necessary to go out of and reenter the impulse noise mode.

5.186 When IMPULSE COUNTER switch S17 is set at CONT (CONTINUOUS), the divide-by-6000 circuit is disabled. The time-left counters cannot be clocked and TIME OUT remains low.

5.187 IMPULSE NOISE MEASUREMENT DETAILED DESCRIPTION

5.188 LEVEL COMPARATORS (Figure 7—32)

5.189 Precision divider R79-R89 provides six voltages used as comparator thresholds. The low level comparator U7 threshold is fixed at +0.50 volts. Two of the other five voltages are selected in each position of THRESHOLD SEPARATION switch S16D3 to provide medium and high level thresholds. Switches Q30 and Q27 are closed in the 2-dB position, Q29 and Q26 in the 4-dB position, and Q28 and Q25 in the 6-dB position. Diodes limit each comparator output at logic low and high levels. A positive-going output pulse is produced for each input exceeding a threshold. Note that a pulse from the high level comparator is accompanied by pulses from the lower comparators. A pulse from the medium level comparator is accompanied by a pulse from the low level comparator. Outputs are connected to logic board A through logic board B.

5.190 RATE LIMITERS AND EVENT COUNTERS (Figure 7—28)

5.191 The high level rate limiter includes U29A and binary counter U30A. In the quiescent state, U29A is reset and U30A is cleared. The 100-Hz clock at U30-2 is defeated by the high at U30-1. A HI LEVEL pulse sets U29A. The 100-Hz clock is enabled. After seven counts, U31-6 goes low and U24-3 goes high. The D flip-flop and counter are cleared by the output from U24-3. The output of U31A feeds the clock gate of the lowest order stage in the high level event counter. The interval between the HI LEVEL input pulse and the appearance of the clock pulse from U31A is 600 to 700 milliseconds. Additional HI LEVEL pulses in this interval are not sensed by this circuit.

5.192 The high level event counter includes decade counters U10 and U19. The clock gate U32A accepts the rate limiter output unless defeated by TIME OUT

or the output of U23A, which goes high when the count reaches 9999. Gates detect the count of 9 at the output of each stage. When the count advances from 9 to 0, the low-to-high transition from the gate clocks the next higher stage. When 9 is contained in each of the our stages, U23A is conditioned to defeat the rate limiter output. The counter contents are thus frozen at 9999. The BCD output of each stage is gated by display selection controls applied to transmission gates U4, U5, U13, and U14.

5.193 The medium and low level rate limiters and counters are identical to the high level circuits.

5.194 DELAYED RELEASE CIRCUIT (Figure 7–28)

5.195 The delayed release circuit includes U29B and binary counter U30B. When not in impulse noise mode, U30B is held reset. The high $\overline{\text{ENABLE}}$ signal holds all event counters reset. Divider U29B operates continuously, but it can not clock U30B with MR held high. When the impulse noise mode is activated, reset is released from U30B. The 20-millisecond square wave from U29B now clocks U30B. The eight high-to-low transition sets U30B-Q3 output. The event counters are now released. Also, the clock to U30B is defeated by the high at U30-9. The delay is 140 to 160 milliseconds.

5.196 DIVIDE-BY-6000 CIRCUIT (Figure 7–30 Sheet 1)

5.197 The divide-by-6000 circuit is in its quiescent state when the test is not in impulse noise mode. The $\overline{\text{IMP NOISE}}$ control function at U19-8 holds binary counter U22 reset. In this state, U23-3 is low and the 100 HZ clock holds U15B cleared. The ONE-MINUTE CLOCK is static. When in the impulse noise mode, the reset is released from U22, which is then clocked by the 100-HZ input. Gates U21A, U21B, and U23A detect the count of 6000. The next 100-HZ clock sets U15. The ONE-MINUTE CLOCK clears U22 and the next 100-HZ clock clears U15B. Another cycle starts. When IMPULSE COUNTER switch S17 is at CONT, the signals holds U15B set. The ONE-MINUTE CLK is held high and is thus defeated.

5.198 TIME LEFT COUNTER AND TIME OUT DETECTOR (Figure 7 – 30 Sheet 1)

5.199 When not in impulse noise mode, the time-left counter is loaded with BCD data from TIME thumbwheel switches S16D4 and S16D5. The $\overline{\text{IMP NOISE}}$ control signal at U10-1 and U20-1 permits loading without clocks. When impulse noise is active, the switches are disconected. If in the TIMED condition, the counter will be clocked. The UP control input of each counter stage is grounded to permit downward counting only. The counter BCD outputs are available for display via transmission gates U11 and U16.

5.200 When the count decrements from 01 to 00, the low Co outputs produce a high at U19-3. The next 100-HZ clock clears U15A to produce TIME OUT. The TIME OUT signal detects the ONE-MINUTE CLK at U19B and halts accumulation of data by event counters on logic board A. The count of 00 is retained in the time left counter. Thus, U15A can be set only by deactivating impulse noise mode (**i.e.**, by setting IMPULSE COUNTER switch S17 at OFF/RESET or by setting FUNCTION switch S9 at LEVEL or FREQ).

5.201 **DISPLAY SECTION FUNCTIONAL DIAGRAM (FIGURE 7–9)**

5.202 Data from measurement circuits are collected digit-by-digit. The update (scan) rate is 450 times per second. Certain conditions require blanking.

- ☐ The first two leading zeroes are blanked.
- ☐ The fourth digit is blanked in noise measurement modes.
- ☐ The entire digit display is blanked when
  - the input signal level is beyond the upper or or lower auto-ranging limit in level or noise measurement modes,
  - the input signal frequency is beyond the upper limit of frequency measurement in frequency measurement mode, or
  - the input noise level is less than 0 dBrn in circuit noise or noise with tone mode.

The polarity indicator shows the polarity of input signal level and flags certain measurement conditions when accompanied by a blank digit display.

- ☐ The appearance of + indicates that the level exceeds the upper measurement limit in level or noise measurement modes.
- ☐ The appearance of – indicates that the input level lies below the lower measurement limit in level or noise measurement mode, or that for circuit noise or noise with tone measurement the input noise level is below 0 dBrn.

5.203 Clock generator U65 on digital board A3 produces a 1.8-kHz rectangular wave as the scan clock. This clock is converted to a four-phase clock (SCAN

DIGIT A-D). When blanking is not required, SCAN DIGIT A-D pass through blanking gates U71 and U72 on A3 and drivers Q5, Q4, Q15, and Q13 on A8 to the digital display. These signals enable the four segment indicators in sequence. The SCAN DIGIT A-D signals also connect to logic board B through A3XA15 and A7J1 and thence through logic board B to logic board A through A7XW3 and A6XW3.

5.204 Transmission gate A7U1 passes SCAN DIGITS A-D as DIGIT SEL A-D when not in impulse noise mode. These are made available to digital board A3 via A7J1 and A3XA15. Transmission gates A3U48-51 pass BCD data from the four-stage counter an A3 in level and noise measurement modes.

5.205 Transmission gate A7U2 is enabled in impulse noise mode when switch S4 is at TIME LEFT. Transmission gates A7U3, A7U11, and A7U16 pass the time left BCD data from the time left counter. Note that transmission gate A7U3, enabled by SCAN DIGIT A and SCAN DIGIT B, passes only zero.

5.206 Input transmission gates A6U1, A6U2, or A6U3 are enabled in impulse noise mode when switch S4 is in HI, MED, or LOW position, respectively. The enable gate passes SCAN DIGITS A-D to a set of four output transmission gates. One set of gates is provided for each four-stage impulse noise event counter.

5.207 The selected digit is made available to the remote display via A7XW1, to the non-zero detector A3U68A/U59A, and to the BCD-to-segment decoder A8U1. The seven decoder outputs are applied to the four digit indicators in parallel through drivers Q6-Q12. Only the indicator selected by SEL A-D will display the active datum.

5.208 Non-zero detector A3U68A/U59D feeds the sequential blanking circuit. Each scan cycle starts with the sequential blanking circuit set to blank digit A. When SCAN DIGIT A selects a datum equal to zero, the non-zero detector fails to reset the circuit and digit A does not reset the circuit and digit A is blanked out. If SCAN DIGIT B also selects a datum equal to zero, digit B is also blanked out. In either case a non-zero datum resets the sequential blanking circuit to permit display. Digits C and D can not be blanked sequentially. Digit D is always blanked in noise measurement modes.

5.209 Each scan cycle starts with 0.0 dBm detector A3U64 set to blank the polarity indicator. The first scanned non-zero datum defeats the circuit and permits polarity display.

5.210 The second input to A3U62B controls blanking for conditions described in paragraph 5.202.

5.211 In the level measurement mode, the decimal point (DP) in A9U5 and the DBM indicator A9CR3 are activated. In frequency measurement mode, the decimal point in A9U4 and the KHZ indicator A9CR1 are activated if in the KHZ measurement range. When FUNCTION switch S9 is in one of the noise positions and impulse noise is not active, the dBrn indicator A9CR2 is activated. In impulse noise mode, IMPL indicator A9CR4 is activated.

5.212 DISPLAY SECTION DETAILED DESCRIPTION (FIGURE 7—19, SHEET 2)

5.213 SCAN CLOCK AND FOUR-PHASE CLOCK

5.214 A 1.8-kHz rectagular wave is generated by U65. Frequency and duty cycle are set by the associated resistor-capacitor network. The SCAN CLOCK triggers the input stage of divide-by-four circuit U66. The outputs of U66 are illustrated in Figure 5—9. Binary decoder U53A converts divider outputs to a four-phase clock (SCAN DIGITS A-D). The output of U53A is enabled only during the low interval of SCAN CLOCK.

5.215 DIGIT SELECTION

5.216 The SCAN DIGIT outputs of U53A are connected to blanking gates U71A-D. In the absence of a blanking requirement ($\overline{\text{BLANK}}$ high), the SCAN DIGIT outputs are passed to display driver (A8) as $\overline{\text{SELA}}$ - $\overline{\text{SELD}}$. These outputs are inverted by drivers Q5, Q4, Q15, and Q13 on A8 (Figure 7—32). The SELA - SELD outputs of A8 enable A9U2-U5 (Figure 7—34).

5.217 BLANKING

5.218 Latch U69C/D is set at the beginning of each scan cycle by the low outputs from U66-2 and U66-12 and by the low signal from U59D. Gate U68A detects the all-zero condition on data lines 2^0 - 2^3. Inverter U59D thus provides a high for the non-zero condition. Figure 5—9 shows that SCAN DIGIT A is not high at the moment U66 is clocked to the digit A code. Thus, the data lines read zero and U59-11 is low. The latch is set with U69-2. The input of U69-1 is low because U70-13 is high (neither SCAN DIGIT A nor SCAN DIGIT B is high). The high at U69-3 produces a low $\overline{\text{BLANK}}$ signal. The blanking gates are not conditioned when SCAN DIGIT A becomes active, data appears on lines 2^0-2^3. If the data is 0, U59-11 remains low and the latch remains set. Digit A is blanked. Digit B may be simialrly blanked. If the data is non-zero,

U59-11 resets the latch and thus causes the $\overline{\text{BLANK}}$ signal to go high. A low remaining of U59-11 during digit C time does not produce blanking because the low at U70-4 inhibits U69A.

5.219 The $\overline{\text{CN} + \text{NWT} + \text{NTG}}$ input produces a low at U69-5 during SCAN DIGIT D. The input to U69-2 is low at this time because U70-4 is high. Thus, digit D is blanked in these modes.

5.220 Non-sequential blanking signals are applied to U63-5. Blanking is effected by serveral conditions.

- An input signal frequency beyond the upper frequency measurement limit in frequency measurement mode produces a low at U67-10, resulting in a high at U63-5 via U67B.
- Input level exceeding the upper measurement limit in level or noise measurement mode produces a high at U63-11, resulting in a high at U63-5 via U63A and U67B. This condition also activates both segments of the polarity indicator.
- Input level below the lower measurement limit in level or noise measurement mode produces a high at U63-10, resulting in a high at U63-5 via U63A and U67B. This condition also activates the horizontal segment of the polarity indicator.
- Input noise below 0 dBrn in circuit noise or noise with tone modes produces a high at U63-10, resulting in a high at U63-5 and an active horizontal segment of the polarity indicator.

5.221 POLARITY INDICATOR

5.222 In addition to activation of this polarity indicator in association with blanking as described in paragraph 5.219, crossover in level measurement mode effects the display. Also, the polarity indicator is blanked when the measurement result is 0.0 dBm in level measurement mode.

5.223 Tone level measurements in ranges 6 and 7 can yield results either above or below 0.0 dBm. When the result is greater than 0.0 dBm, the PE pulse sets U61B. The Q output of U61B activates the vertical segment of the polarity indicator in this condition. The flip-flop remains set until a measurement result is negative (crossover occurs) or until leaving level measurement mode. The signal at A3XW1-5 is OR-ed with that at A3XW1-1 on display driver board A8. Similarly, the signal at A3XW1-7 is OR-ed with the T control function on A8.

5.224 Blanking of the polarity indicator occurs in level measurement mode when the measured signal power is 0.0 dBm. Johnson counter U64 detects this condition. In the absence of non-zero data, the counter is clocked by SCAN CLOCK until the Q4 output goes high. The high blanks the polarity indicator and inhibits the SCAN CLOCK input. This condition is retained until a non-zero datum is detected. That datum resets U64.

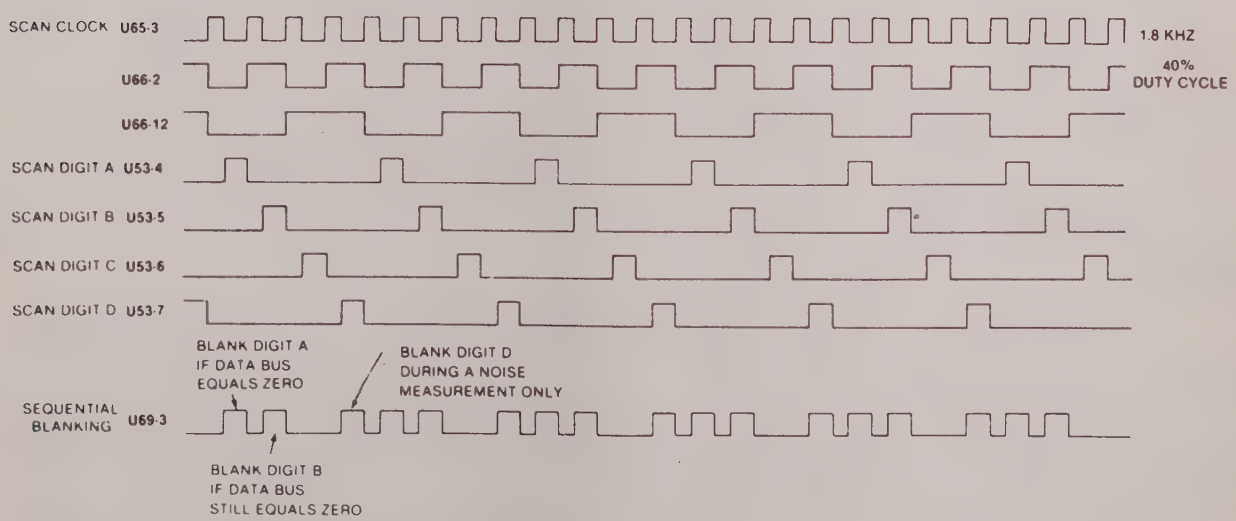


Figure 5—9. Digit Scan Timing Diagram.

5.225 **MODE CONTROL FUNCTIONAL DIAGRAM (FIGURE 7—10)**

5.226 The mode control logic, while easily understood, is not easily traced through the various schematics. Figure 7—10 groups scattered control logic circuits.

- ☐ When FREQ switch S14B or MON SEND FREQ switch S11 is activated, frequency measurement mode is selected independently of the position of FUNCTION switch S9.
- ☐ Mode control does not distinguish between circuit noise (CN) and noise with tone (NWT). Other sections of FUNCTION switch S9 change parameters of receive section circuits on A4 between these positions.
- ☐ The lower input to A7U18D is low unless set high by IMPULSE COUNTER switch S17 in OFF/RESET position. Thus selection of CN, NWT, or NTG with FUNCTION switch S9 enables impulse noise mode at A7U18D unless IMPULSE COUNTER switch S17 is at OFF/RESET. Note that the signal at IMPULSE COUNTER S17 wiper is CN + NWT + NTG.
- ☐ The IMP NOISE control signal from A7U6C has several effects.
  - The IMP 2 signal enables switch S4 and thus permits selection of impulse measurement data for display.
  - The output of A7Q1 activates the IMPL LED.
  - Gate A7U13C defeats A7U13B/D to de-activate the dBrn LED.
  - Gates in A7U9 passes FUNCTION switch positions CN or NWT as being NOISE unless IMP NOISE is active.
  - A gate in A7U17 passes CN + NWT + NTG if IMP NOISE is not active.
  - A second gate in A7U17 modifies F as IMP + F. This signal is used by blanking circuits on A3.

5.227 **POWER SUPPLY AND DISTRIBUTION FUNCTIONAL DIAGRAM (FIGURE 7—11)**

5.228 The Model 4002 Test Set operates from a 115- or 230-vac primary source or from batteries. Batteries BT1-3 are connected through fuses A2A1F1-3 to contacts of relay A2A1K2. Relay A2A1K2 is energized initially by the charging current of C13 produces when S1 is closed. Note, however, that the normally-closed contact of A2A1K1 at A2A1F1 output will be open when the voltage regulators are active. Thus, when the test set is turned on with ac primary power applied, the batteries are switched out. Also, the batteries are supplied with charging currents when operating with an ac input.

5.229 Three other sets of contacts of A2A1K1 select voltage regualtor or battery outputs. Output voltages and ground are distributed as shown.

5.230 The active power source is selected by CR13-16 to supply precision voltage regulators on analog board A4. The precision output voltages are used to establish accurate measurement reference points for circuits on A3 and A8 and operating references for the battery charging regualtors and the battery under-voltage sensor on A2A1.

5.231 The battery under-voltage sensor allows A2A1K2 to remain energized in battery mode unless an overload condition is detected on any of the three battery supply lines.

NOTE

The rack-mounted Model 4002R test set does not operated on an external battery pack. The following paragraphs describe the Model 4002 test set power supply assembly. For the Model 4002R test set, disregard descriptions of the charging circuits, the battery on/off control, and the battery under-voltage sensor. These circuits are inoperative although present.

5.232 **POWER SUPPLY DETAILED DESCRIPTION**

5.233 AC OPERATION (FIGURE 7—17)

5.234 With the test set connected to an ac source, voltages from the transformer/rectifier are supplied to the voltage regulators and the charging circuits. Neither the voltages from the voltage regulators nor from the batteries are available on the outputs of the power supply for use by the circuit boards within the test set with S1 at OFF.

5.235 However, the +12V and −12V outputs from the voltage regulators do go to a +5V precision regulator via diode gates CR14-CR17. The outputs from the precision regualtor serve as reference voltages for the charging circuit and the under-voltage sensor circuit.

5.236 With POWER switch S1 at ON, the regulated voltage sensor monitors the +5V and −12V outputs and operates sensor relay K1 if the test set is connected to an ac source. Operated sensor relay K1 allows only

the +5V, +12V, and −12V outputs from the voltage regulators to be distributed within the test set.

5.237 **Transformer/Rectifier**

5.238 A 115/230 slide switch (A2S15) allows transformer T1 to be connected to either a 115-Vac or 230-Vac source. Transformer T1 applies two 20 Vrms voltages to diode bridge CR1-CR4 and one 12 Vrms voltage to diode bridge CR5-CR8. The rectified voltages are filtered by capacitors C1, C2, and C3.

5.239 **Voltage Regulators**

5.240 Voltage regulators VR1, VR2, and VR3 are three-terminal devices which supply −12V, +12V, and +5V respectively. The positive voltage regulators have ground connected to the case, while the negative voltage regulator has the input unregulated voltage connected to its case.

5.241 **Regulated Voltage Sensor**

5.242 The regulated voltages sensor simply consists of relay K1. With POWER switch S1, the relay operates only if both the +5V and −12V from the voltage regulators are present. This indicates that the test set is connected to an ac source. Operated relay K1 also prevents the battery on/off relay K2 from operating.

5.243 BATTERY OPERATION (PORTABLE SETS ONLY) (FIGURE 7−17)

5.244 If the test set is not connected to an ac source, then setting POWER switch S1 to on operates on/off relay K2. Operated on/off relay K2 allows the +5V, +12V, and −12V battery voltages to be distributed via the normally closed contacts of sensor relay K1. An undervoltage sensor releases K2 should the voltage of any one battery fall below a critical threshold. Cutting off the battery voltages ensures that the test set does not operate with inefficient voltages and protects the batteries against deep discharges.

5.245 **Charging Circuits**

5.246 Three constant voltage sources provide battery charging currents. All three sources operate in a similar manner and only the +12V circuit will be described. Amplifier U1 and power transistor Q1 (T1P29A) form a non-inverting amplifier which uses the +5V precision voltage to supply +14.6V at the junction of resistors R1 and R2. When charging is nearly completed the current is low and voltage drop across resistor R1 is negligeable. Therefore the voltage at the cathode of diode CR9 is 14.0V assuming a 0.6V drop across the diode. The 12-volt battery is fully charged when the voltage across itself is between 13.8V and 14.4V.

5.247 Capacitor C10 prevents high-frequency oscillations. Transistor Q1 and resistor R1 limit the inital charging current to 175 mA. Power transistor Q1 (T1P29A) increases the current sourcing capability of amplifier U1. The batteries are a gelled electrolyte (lead-dioxide) type and require no maintenance.

5.248 **Battery On/Off Control**

5.249 Assume that the test set is not connected to an ac source and the battery pack is connected. Relay K1 remains released (no outputs from the voltage regulators) when POWER switch S1 is set at ON. The charging current through capacitor C13 operates on/off relay K2. With K2 operated, transistor Q4 turns on to latch the relay and apply the +12V, −12V, and +5V batteries to the test set via the normally closed contacts of relay K1. On/off relay K2 remains energized until the POWER switch is set to off or until transistor Q5 cuts off transistor Q4. Transistor Q5 is momentarily turned on by the undervoltage sensor when a low voltage conditon is detected.

5.250 Setting the POWER switch at off, connects resistor R10 to quickly discharge capacitor C13. This enables the test set to be turned on again quickly. The test set cannot turn itself back on again when shut off by an undervoltage condition since capacitor C13 is charged and blocks the dc current to on/off relay K2.

5.251 **Battery Undervoltage Sensor**

5.252 The battery undervoltage sensor consists of transistors Q6 through Q9 with associated resistors. With the batteries charged, transistors Q7, Q8, and Q9 are cut off and transistor Q5 has no effect on the on/off control. For the −12V battery voltage, transistor Q9 turns on when its base voltage is 0.6 to 0.7 volts. This occurs when the voltage across resistor R22 is 4.4 to 4.3 volts which corresponds to a battery voltage of −10.6 to −10.2 volts. Therefore, transistor Q9 turns on transistor Q5 to shut the test set when the −12V battery voltage is smaller than −10.4 volts.

5.253 Transistors Q7 and Q8 operate in a similar manner except that they turn on transistor Q5 via inverter Q6. Transistor Q6 has a +10.4-volt threshold to monitor the +12V battery voltage. Transistor Q7, monitoring the +6V battery voltage, has a +4.5-volt threshold.

5.254 PRECISION REGULATOR (FIGURE 7—22)

5.255 The dual precision regulator is mounted on the analog board. Each regulator includes an error amplifier and series regulator. The positive regulator is a conventional voltage regulator using the +12V battery voltage. Zener diode VR1 and voltage divider R254/R255 supply a +3.2V reference voltage to error amplifier U29. The error amplifier monitors the output with respect to ground via voltage divider R257/R265/R258 to maintain the output at +5 volts. Resistor R265 can set the output voltage between +4.6 and +5.6 volts. Transistor Q43 and resistor R256 limit the output current to a maximum value of 60 mA.

5.256 The negative regulator operates in a similar manner except that error amplifier U30 uses ground as a reference and monitors the −5V output with respect to the +5 volt output. Therefore, any change on the positive output is reflected as an equal but opposite change on the negative output. Thus, the negative regulator tracks the positive regulator.

5.257 REMOTE DISPLAY SIGNALS

5.258 Remote display signals are available to XW1 and XW2 on logic board B (A7). The signals on these pins are listed in Table 5—2.

Table 5—2. Remote Display Signals

	PIN	SIGNAL	DESCRIPTION
A7XW1	1	TONE	Tone level measurement
	2	FREQ	Frequency Measurement
	3	NOISE	Circuit noise or noise with tone measurement
	4	OVER	Level or noise above measurement limit
	5	PE	Data counter preset enable
	6	+LED	Sign of level measurement or measurement limit
	7	co2	Carry out from next to MSD data counter stage
	8	co1	Carry out from MSD data counter stage
	9	2^1	Data, bcd digit bit weight 2
	10	2^3	Data bcd digit bit weight 8
	11	2^0	Data, bcd digit bit weight 1
	12	2^2	Data, bcd digit bit weight 4
	13	DATA STREAM	Gated VCO
	14	PPL OR	Frequency exceeds limit of phase locked loop circuit
	15	BLANK	Suppress data - digit is a leading zero or an out of range condition exists.
	16	NTG	Noise-to-ground measurement

	PIN	SIGNAL	DESCRIPTION
A7XW2	1	A	Digit strobing signals, MSD
	2	C	Digit strobing signals, MSD
	3	B	Digit strobing signals, MSD
	4	D	Digit strobing signals, LSD
	5	± BLANK	polarity blanking control
	6	TP9	not used
	7	KHZ/HZ	frequency range status
	8	100 HZ	data validation clock
	9	UNDER	Level or noise below measurement limit
	10	TP11	Not used
	11	TP10	Not used
	12	IMPL	Impulse noise measurement
	13	SCAN DIGIT D	Not used
	14	SCAN DIGIT B	Not used
	15	SCAN DIGIT C	Not used
	16	SCAN DIGIT A	Not used

SECTION 6

MAINTENANCE

6.1 This section contains information needed to calibrate the Model 4002 Transmission Test Set.

6.2 FUSES

6.3 The test set contains five fuses. Table 6—1 lists the fuses, their locations, and their functions.

Table 6—1. Fuses

LOCATION	FUSE	FUNCTION
Rear Panel	F4, F5	Protects against excessive ac current. Use a 0.3A slow blow fuse for 115 Vac operation. Use a 0.2A slow-blow fuse for 230 Vac operation.
Power Supply Assembly	F1, F2, F3, 2 Amp	Protects against excessive battery drain.

6.4 The ac input fuses are accessible at the rear panel. The other fuses are accessible after removing the top and bottom covers.

6.5 TEST SET CALIBRATION

6.6 The following paragraphs provide a complete set of adjustment procedures for the test set. These procedures can be used for periodic maintenance or after repair of the test set. These procedures require precision laboratory test equipment. Personnel performing these procedures must be familiar with the type of test equipment specified. No attempt to calibrate this test set should be made without the proper test equipment or qualified personnel.

6.7 TEST EQUIPMENT REQUIRED

6.8 Table 6—2 lists the equipment required to calibrate the test set. If the recommended equipment is not available, use a substitute that can meet the requirements listed in Table 6—2.

6.9 In addition to the commercially available test equipment, the test set requires two special circuits. One circuit monitors the "hundredth" digit and the range status. The other circuit generates pulses used when aligning the impulse noise measurement circuit.

6.10 Figure 6—1 shows the schematic of a suggested monitor circuit. All electrical components are specified but no physical configuration is given. The need to easily see the display after connecting the monitor circuit to the test set must be kept in mind when designing the monitor circuit. The monitor circuit does not require an external power since it obtains power from the test set.

6.11 Figure 6—2 shows the schematic of a possible impulse test circuit. Only the electrical components are specified. Any convenient physical configuration should suffice. This impulse test circuit could be replaced with a pulse generator which outputs a 1-millisecond pulse when triggered by another signal generator every 200-milliseconds.

6.12 PREPARATION FOR CALIBRATION

6.13 Preparation for calibration consists of removing the test set from its enclosure to expose all adjustments. Figure 6—3 and 6—4 show the adjustment locations. Before beginning any alignment, all test equipment should be allowed to warmup for the period specified by the test equipment manufacturers.

6.14 Preparing Model 4002 Test Set

1. If the battery pack is attached, then disconnect and remove the battery pack.

2. If the front panel cover is on, remove it.

3. Loosen and remove the three sets of screws and washers on each side of the test set.

4. Remove the top and bottom covers.

5. For safekeeping, the screws and washers may be loosely secured on the chassis.

6. Stand the test set right side up.

7. Remove the two fuses from the rear panel.

8. Loosen and remove three sets of screws and washers holding the power tray to the chassis.

9. Loosen and remove three screws on each side of the chassis. These screws hold the power tray secured to the chassis.

10. Carefully remove the power tray out of the chassis as follows:

a. Place the test set so that the rear of the chassis faces you.

b. Lift up the right side of the power tray to clear the screws securing the heatsink.

c. Push the power forward while at the same time lift up the rear of the power tray to clear the battery connector past the rear panel.

d. Ensure that all cables remain connected to the printed circuit boards in the power tray.

11. Place the chassis on its left side with the power tray still electrically connected to the chassis.

12. For testing convenience, the power tray may be physically attached to the chassis as shown in Figure 6–5.

13. For safekeeping, the remaining screws and washers may be loosely secured to the power tray.

14. Check that the fuses (removed in step 7) are the proper fuses for the ac source to be used (refer to Table 6–1).

15. Replace the fuses in the test set.

16. Ensure that the rear panel 115/230 switch is set for the ac source to be used.

17. Connect an ac source to the test set.

18. Connect the ".01 digit" IC test clip of the range and .01 digit monitor test circuit to U42 on logic board A3 and the alligator clip to TP 13 on A3. Ensure that pin 1 of IC test clip goes on pin 1 of U42.

19. Connect the "range" IC test clip of the range and .01 digit monitor test circuit to U42 and A3. Ensure that pin 1 of the IC test clip goes on pin 1 of U17.

20. Set test set POWER switch at ON and observe that both the "range" and the ".01 digit" displays light up. If neither display lights up, turn the test set off and repeats steps 18, 19.

6.15 Preparing the Model 4002R Test Set

1. Disconnect the power cord and any other connections present on the rear terminal block.

2. Loosen and remove the six sets of screws and washers on the front panel. These screws secure the test set chassis to the mounting case.

3. Pull the test set chassis out of the mounting case.

4. Loosely secure the screws and washers back on the mounting case for safekeeping.

5. Proceed with step 6 of paragraph 6–14.

6.16 RECEIVE SECTION CALIBRATION

6.17 The receive section calibration is presented as a series of check and adjustment procedures for easy reference. The entire series of procedures must be performed in the order presented since most of the procedures depend upon the adjustments made in previous procedures. In addition, the procedures assume that positions of the switches and controls remain in their previously specified positions unless specifically instructed to set at new positions. Where no tolerances are given, then every attempt should be made to obtain exactly the specified value.

6.18 +5V Reference Check and Adjustment

1. Connect the digital volt meter to +5V test point 41 and test point 38 on the analog board.

2. Set POWER switch on test set at ON and allow serveral minutes for warm-up.

3. The voltmeter should read $+5.00 \pm 0.01$V. If necessary, adjust potentiometer R265 on analog board.

4. Disconnect the digital voltmeter.

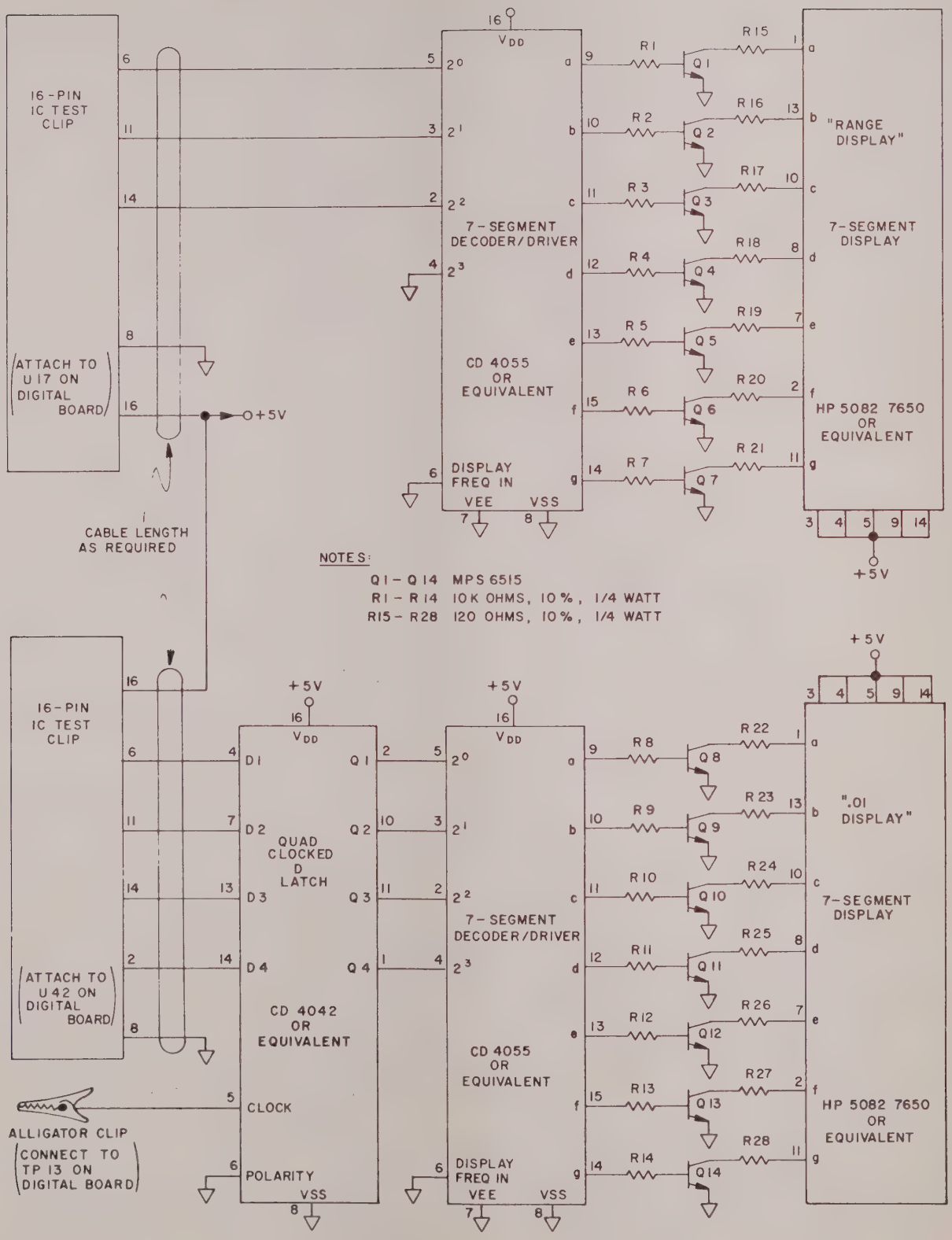


Figure 6—1. Range and 0.01 Digit Monitor Circuit.

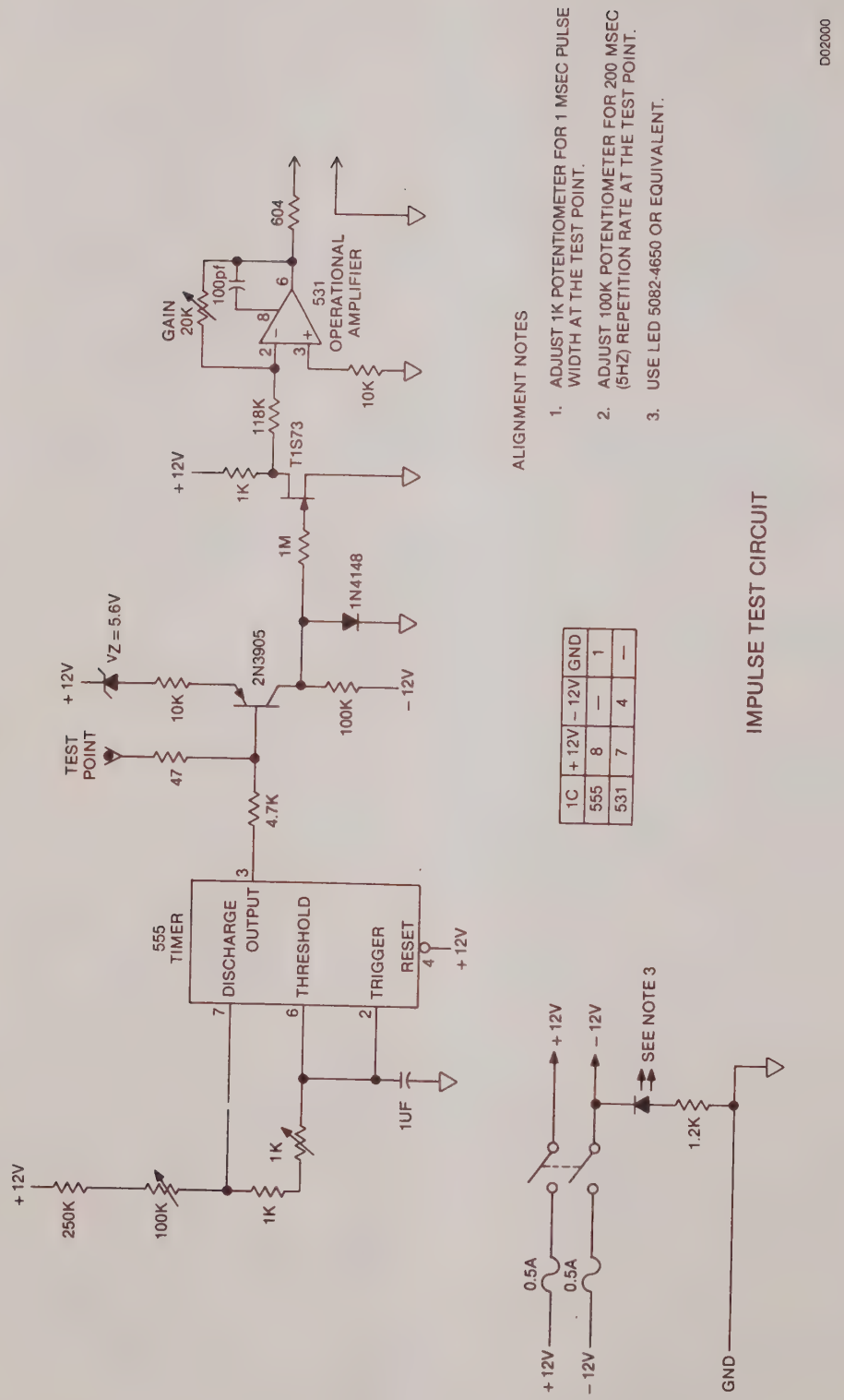


Figure 6—2. Impulse Test Circuit.

Table 6—2. Test Equipment

EQUIPMENT	USE
Digital Voltmeter, Hewlett Packard Model 3465A or equivalent	To adjust +5V reference with an accuracy of ±10 millivolts.
Frequency Counter, Hewlett Packard Model 5328A or equivalent	To adjust 100.00 Hz clock with an accuracy of ±0.0001 Hz.
AC Calibrator, Hewlett Packard Model 745A or equivalent	To supply accurate input level to test set when aligning receive section. Calibrator must be settable to six places (1 part per million). Input level requirement ranges from 6 Vrms to 150 uVrms.
Distortion Analyzer, Hewlett Packard Model 334A or equivalent	To measure distortion when aligning the send section. Analyzer must measure 0.3% distortion at 1 kHz with an accuracy of ±3% or better.
General purpose oscilloscope	To observe waveforms when aligning the impulse noise measure circuits.
Attenuator (0.1 dB resolution)	To vary the output of the impulse test circuit.
Precision Resistors 900 ohms, 0.01% 600 ohms, 0.01% 135 ohms, 0.01%	To pad the output of the ac calibrator thus presenting the test set with an accurate source impedance.
Range and 0.01 Digit Monitor (See Figure 6—1)	To observe the range status and the fifth (LSD) digit.
Impulse Test Circuit (See Figure 6—2)	To supply a test signal when aligning the impulse noise measure circuits.

6.19 **Frequency Check and Adjustment**

1. Connect a precision 900-ohm resistor (0.01%) between the ac calibrator HI OUTPUT jack and the test set LINE A T jack. Connect the ac calibrator LO OUTPUT jack to the test set LINE A R jack.

2. Connect ac calibrator COUNTER OUTPUT rear connector to frequency counter INPUT jack.

3. Set the test set switches as follows:

HOLD A + B	OFF
RECEIVE IMPEDANCE (DIAL)	900
LINE SELECT	SEND B REC A
FUNCTION	FREQ
TERM/BRDG	TERM

4. Set the ac calibrator output level at 6.00000V.

5. Slowly change the ac calibrator output frequency from 20 Hz to 60 kHz. The test set digital display should agree with the frequency counter reading. The digital display least significant digits must agree within ±2 with the corresponding frequency counter digit.

6. If correct results were observed in the previous step, then the test set time base does not require adjustment; proceed with the logger check and adjustment (paragraph 6.20). If incorrect results were obtained, proceed to step 7.

7. Connect frequency counter to the 100 Hz test point on digital board A3.

8. Adjust A3C1 to obtain a reading of 10.0000 ± 0.0001 msec on the frequency counter.

9. Reconnect the frequency counter to COUNTER OUTPUT rear connector on the ac calibrator.

6.20 Logger Check and Adjustment

1. Set test set FUNCTION switch at LEVEL.

2. Set the ac calibrator frequency at 1000 ± 1 Hz and the output level at 6.00000V. ("Range" display reads 7.)

NOTE

All digital display readings include the ".01 digit" display (connected to U42 on the digital board) as the last significant digit.

3. Record the reading of the digital display.

4. Lower the ac calibrator output level to 1.89737V. Do not allow the ac calibrator output level setting to go below 1.80000V. ("Range" display remains at 7.)

5. Record the reading of the digital display.

6. Subtract the step 5 reading from the step 3 reading. The difference between the two readings must be exactly 10.00 dB. If necessary, adjust LOG SCALE FACTOR potentiometer R13 on logic board A3 (accessible through a hole on the high hand side of the chassis). Make the adjustment with the input at 1.89737V.

7. Repeat steps 2 through 6 to check the adjustment and readjust if necessary.

6.21 Measurement Window Check and Adjustment

1. Raise the ac calibrator output level to 2.89737V and wait for the digital display to settle. ("Range" display reads 7.)

2. Lower the ac calibrator output level to 1.89737V. ("Range" display remains at 7.)

3. Record the reading of digital display.

4. Lower the ac calibrator output level to 1.09737V and wait for the display to settle. ("Range" display reads 6.)

5. Reset the ac calibrator output level to 1.89737V. ("Range" display remains at 6.)

6. The digital display reading must be identical to the reading recorded in step 3. If necessary, adjust UPPER LIMIT potentiometer R25 on logic board A3. Make the adjustment with the input at 1.89737 volts.

7. Repeat steps 1 through 6 to check the adjustment, and readjust if necessary.

6.22 Level at 900 Ohms Checks and Adjustment

1. Set the ac calibrator output level at 1.09737 mV then at 1.89737 mV ("Range" display reads 0.)

2. The digital display must read −60.05 dBm. If necessary adjust LEVEL CAL potentiometer R129 on the analog board.

3. Set the ac calibrator output level at 6.00000V. ("Range" display reads 7.)

4. The digital display must read +10.05 dBm. If necessary, adjust range 7 LEVEL potentiometer R113 on the analog board (accessible through a hole in the I/O impedance board).

5. Lower the ac calibrator output level to 1.91934V. Do not allow the ac calibrator output level setting to go below 1.90000V. ("Range" display remains at 7.)

6. The digital display must read +0.15 dBm. If necessary, adjust LEVEL tracking potentiometer R138 on the analog board.

7. Repeat steps 3 through 6 unitl no further adjustments are required.

NOTE

Repeat paragraph 6.20, paragraph 6.21, and paragraph 6.22 until no further adjustments are required. When correctly adjusted, the following digital display readings should be obtained:

a. logger step 3: +10.05 dBm
b. logger step 5: +0.05 dBm
c. measurement window step 3: +0.05 dBm
d. measurement window step 6: +0.15 dBm

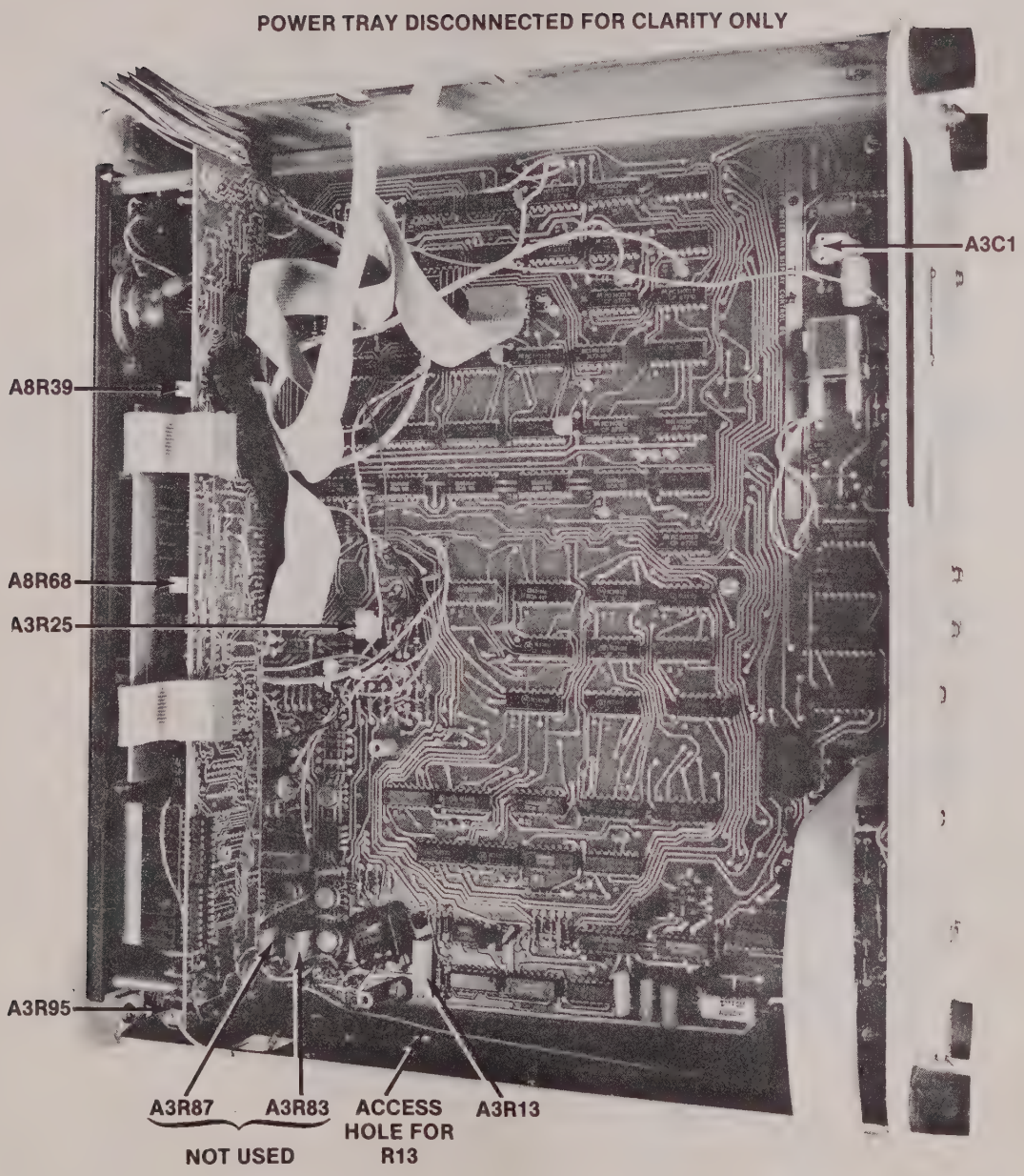


Figure 6—3. Adjustment Locations For Digital Board A3 And Display Driver A8.

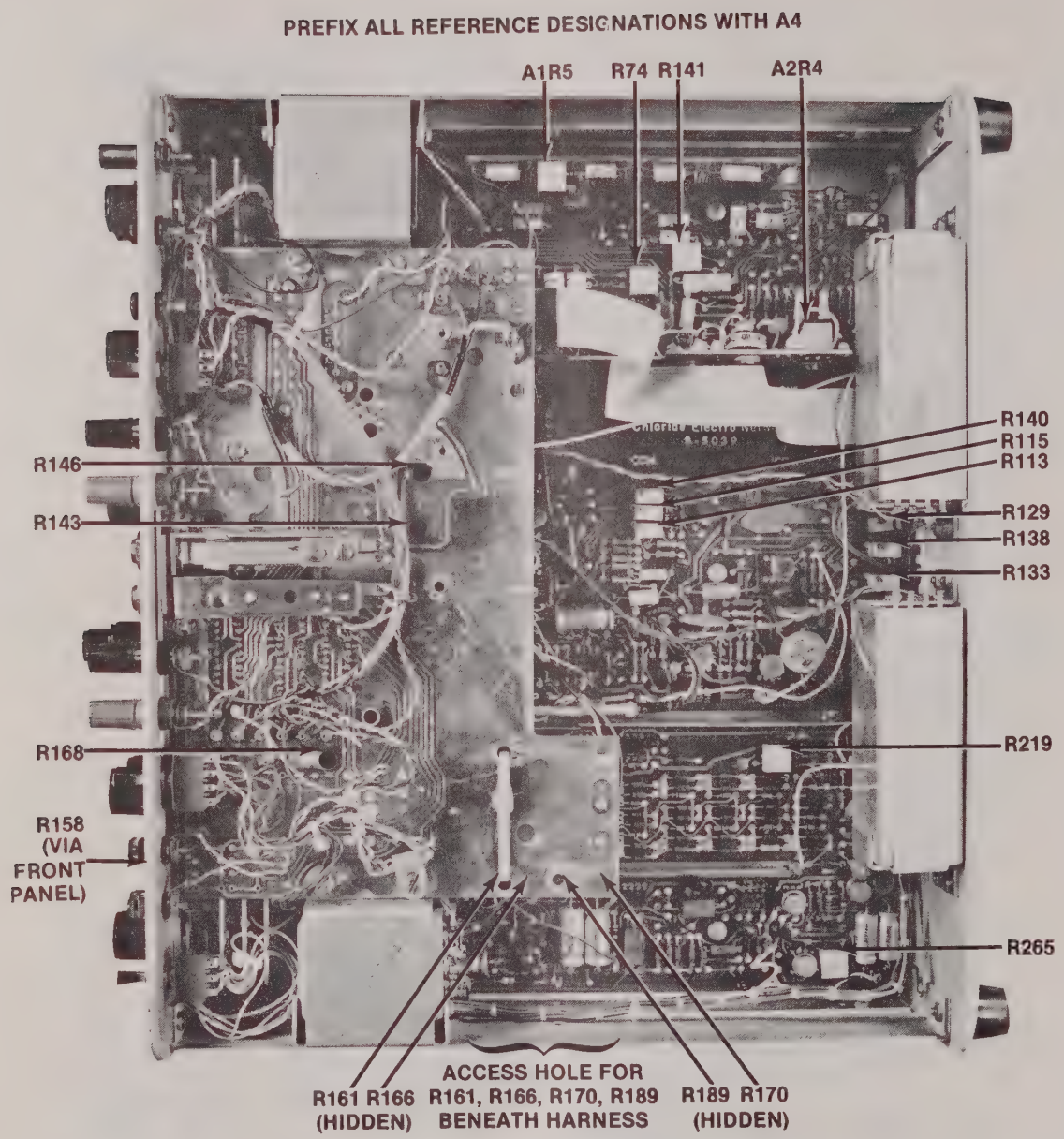


Figure 6—4. Adjustment Locations For Analog Board A4.

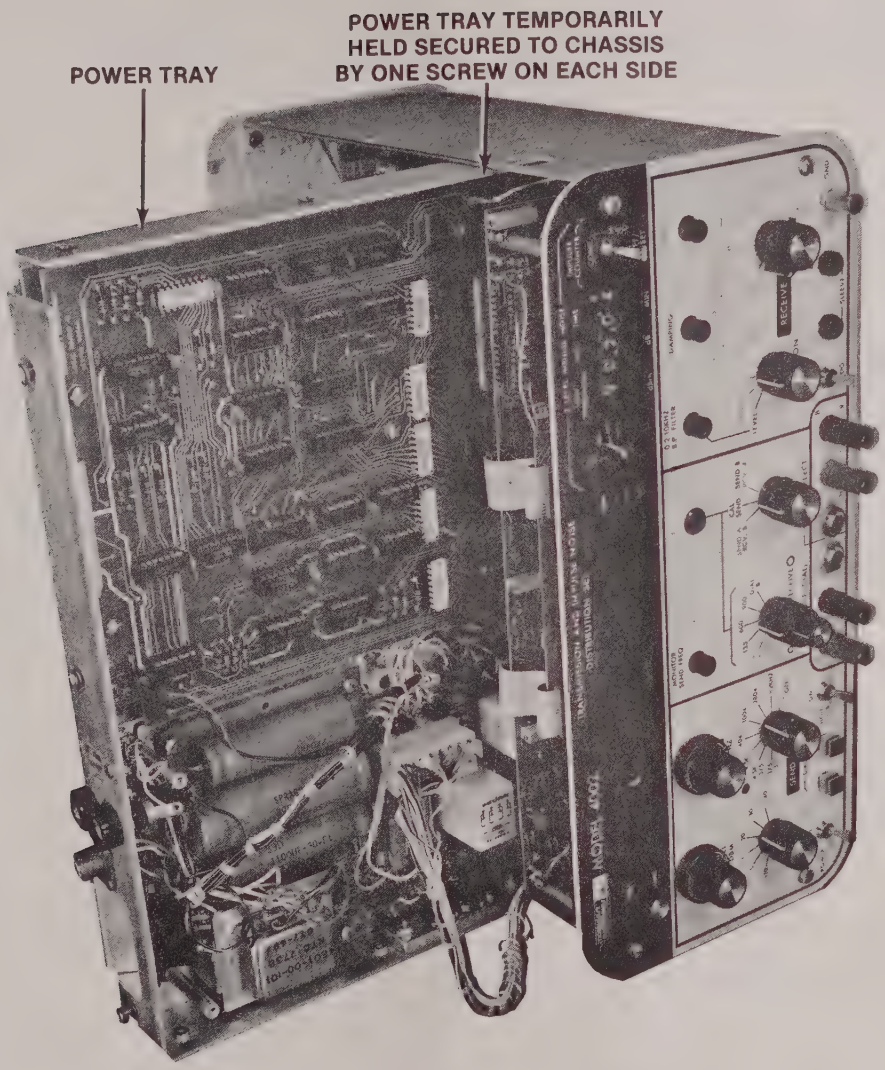


Figure 6—5. Securing The Power Tray To The Chassis.

6.23 Level at 600 Ohms Check and Adjustment

1. Replace the precision 900-ohm resistor connected between the ac calibrator and the test set with a 600-ohm resistor (0.01%).

2. Set the test set RECEIVE IMPEDANCE (DIAL) switch at 600.

3. Set the ac calibrator output level at 4.89898V. ("Range" display reads 7.)

4. The digital display must read +10.05 dBm. If necessary, adjust 600 CAL potentiometer R146 on the analog board.

6.24 Level at 135 Ohms Check and Adjustment

1. Replace the precision 600-ohm resistor connected between the ac calibrator and the test set with a 135-ohm (0.01%) resistor.

2. Set the RECEIVE IMPEDANCE (DIAL) switch at 135.

3. Set the ac calibrator output level at 2.32379V. ("Range" display reads 7.)

4. The digital display must read +10.05 dBm. If necessary, adjust 135 CAL potentiometer R143 on the analog board.

6.25 Bandpass Filter Gain Check and Adjustment

1. Replace the precision 135-ohm resistor connected between the ac calibrator and the test set with a 600-ohm (0.01%) resistor.

2. Set the RECEIVE IMPEDANCE (DIAL) switch at 600.

3. Set the ac calibrator output level at 4.89898V. ("Range" display reads 7.)

4. Hold the B.P. FILTER switch pressed. The digital display must read 10.05 dBm. If necessary, adjust BPF GAIN potentiometer R74 on the analog board.

6.26 Noise Check and Adjustment

1. Set the FUNCTION switch at CKT NOISE, the WEIGHTING switch at 3 KHZ FLAT, the SEND IMPDANCE (DIAL) switch at 600.

2. Set the ac calibrator output level at 0.054919 mV then at 0.154919 mV. ("Range" display reads 0.)

3. The digital display must read 1050±2 dBrn (actually 10.50 but the decimal point does not appear). If necessary, adjust NOISE CAL potentiometer R140 on the analog board (accessible through a hole in the I/O impedance board).

4. Set the ac calibrator output level at 0.489898V. ("Range" display reads 7.)

5. The digital display must read 8050±2 dBrn. If necessary, adjust RO NCAL potentiometer R115 on the analog board (accessible through a hole in I/O impedance board).

6. Set the ac calibrator output level at 0.154949V. Do not allow the ac calibrator output level setting to go below 0.150000V. ("Range" display remains at 7.)

7. The digital display must read 7050±2 dBrn. If necessary, adjust NOISE potentiometer R133 on the analog board.

8. Repeat steps 2 through 7 until no further adjustments are required.

6.27 C-Message Filter Gain Check and Adjustment

1. Set the WEIGHTING switch at C—MSG.

2. Set the ac calibrator output level at 0.489898V. ("Range" display reads 7.)

3. The digital display must read 8050±2 dBrn. If necessary, adjust GAIN potentiometer R5 on the C-message filter board.

6.28 Program Filter Gain Check and Adjustment

1. Set the WEIGHTING switch at PRGM.

2. The digital display must read 8050 dBrn. If necessary, adjust PF GAIN potentiometer R141 on the analog board.

6.29 50 kb/s Filter Gain Check and Adjustment

1. Set the WEIGHTING switch at 50KBIT ("Range" display reads 7.)

2. The digital display must read 8050±2 dBrn. If necessary, adjust 50KBIT GAIN potentiometer R4 on the 50 kb/s filter.

FOR 11/15/93 ONE NOTE

CAUTION
CHANGES HAVE BEE[N] OF
ON THIS PA[GE]
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* NOTE: ON DIGITAL BD. UNSOLDER WIRE GOING TO PIN 10 TO OBSERVE CORRECT DISPLAY RESPONSE WHEN

6.30 Impulse Noise Gain Check and Adjustment

1. Disconnect the ac calibrator output from the test set. Remove the precision 600-ohm resistor connected to the ac calibrator HI OUTPUT jack. Leave the frequency counter connected to the ac calibrator.

2. Connect the digital voltmeter to test point 19 on display driver A8.

3. Observe that the digital voltmeter reads 0 ± 2 mVdc. If necessary, adjust potentiometer A8R95 to obtain 0 ± 2 mVdc at A8TP19.

4. Disconnect the digital voltmeter.

5. Connect the oscilloscope to test point 19 on display driver A8.

6. Set the test set switches as follows:

FUNCTION	CKT
WEIGHTING	15 KHZ FLAT
FREQ HZ	OFF
Thumbwheels:	
LOW THRESHOLD	50
SEP	6
TIME	99
Impulse noise display switch	LOW
IMPULSE COUNTER	OFF/RESET to CONT

7. Connect the output of the "impulse test circuit" to the input of the attenuator.

8. Connect the output of the attenuator to the LINE A T and R jacks.

NOTE

The signal at the test point on the "impulse test circuit" may be used to trigger the oscilloscope.

9. Set the "impulse test circuit" gain at mid range. Adjust the attenuator setting to obtain a convenient trace on the oscilloscope. The waveform amplitude should be as large as possible.

10. Note the waveform amplitude.

11. Reverse the input leads at the test set LINE A T and R jacks.

12. The waveform amplitude should be the same as noted in step 10. If necessary, adjust potentiometer A8R68 to obtain the same amplitude as noted in step 10.

NOTE

If potentiometer A8R68 does not affect the amplitude of the displayed waveform go to step 9 without reversing the test set input leads.

13. Reverse the input leads at the test set LINE A T and R jacks.

14. Repeat steps 10 through 13 until no difference in amplitude can be seen on the oscilloscope.

15. Disconnect the oscilliscope and the attenuator from the test set.

16. Reconnect the ac calibrator output directly (no precision resistor) to the test set LINE A T and R jacks.

17. Set the ac calibrator output level at 5.47723 mV.

18. Set the ac calibrator frequency at 1000 ± 1 Hz.

19. Adjust potentiometer A8R39 until the LOW count register just begins to count.

20. When properly aligned, the test set should "not count" or "count" as specified in Table 6–3. If necessary, repeat steps 17 and 18.

6.31 SEND SECTION CALIBRATION

1. Patch LINE A and LINE B connectors.

2. Connect the distortion analyzer input connector to LINE A connectors.

3. Set test set switches as follows:

LEVEL DBM	+10
FREQ HZ	1004
HOLD A&B	OFF
IMPEDANCE (DIAL)	600 (both switches)
SELECT	SEND A REC B
FUNCTION	LEVEL
TERM/BRDG	TERM

4. Adjust LEVEL DBM poteniometer to obtain 10.0 ± 0.1 dBm on the digital display.

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ON THIS PAGE.
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5. If distortion is 0.3% or less, proceed to step 6. Otherwise proceed as follows. Waveform information in parenthesis relate to fault analysis with an oscilloscope on LINE A connectors. Adjustment with an oscilloscope may produce acceptable output characteristics.

a. Adjust −BIAS potentiometer A3R170 and +BIAS potentiometer A3R189 (accessible through holes on left side of chassis) for best reading (minimum distortion in the 10% to 90% voltage regions).

b. Adjust LEVEL 1 potentiometer A3R166 (accessible through hole on left side of chassis) for best reading (minimum distortion at voltage peaks).

c. Repeat a and b as necessary.

d. Adjust SYMMETRY potentiometer A3R161 (accessible through hole on left side of chassis) for best reading (same interval of positive and negative voltages).

e. Adjust CROSSOVER potentiometer A3R219 for best reading (least distortion at or near zero crossover voltage).

f. Repeat d and e as necessary.

6. Set up send section for +10 dBm at 20.0±0.1 kHz.

7. If distortion exceeds 1.0% adjust FREQ COMP potentiometer A3R168 (accessible through a hole A5).

8. Set FREQ HZ switch 2804, 1004, and 404. Note each reading. If necessary, adjust A3R158 (accessible through hole in front panel) to obtain all readings to within 2 Hz. Adjustment affects the 2804-Hz output to a larger extent than the lower frequencies.

9. De-energize test set.

10. Disconnect test equipment.

11. Replace the power tray and covers.

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Table 6—3. Impulse Noise Alignment Check Points.

AC CALIBRATOR VOLTAGE SETTING AT 1-KHZ		THUMBWHEEL **LOW THRESHOLD**	THRESHOLD **SEP**ARATION	SELECTED COUNT REGISTER	STATUS OF COUNT REGISTER
VOLT	DBRN EQUIVALENT				
0.868082 V	94	95	6	LOW	not counting
1.092850 V	96	95	6	LOW	counting
086.8082mV	74	75	6	LOW	not counting
109.2850mV	76	75	6	LOW	counting
08.68082mV	54	55	6	LOW	not counting
10.92850mV	56	55	6	LOW	counting
0.868082mV	34	35	6	LOW	not counting
1.092850mV	36	35	6	LOW	counting
9.74004mV	55	50	6	MED	not counting
12.2620mV	57	50	6	MED	counting
19.4339mV	61	50	6	HI	not counting
24.4659mV	63	50	6	HI	counting
7.73679mV	53	50	4	MED	not counting
9.74004mV	55	50	4	MED	counting
12.2620mV	57	50	4	HI	not counting
15.4370mV	59	50	4	HI	counting
6.14555mV	51	50	2	MED	not counting
7.73679mV	53	50	2	MED	counting
7.73679mV	53	50	2	HI	not counting
9.74004mV	55	50	2	HI	counting

1. Set **TIME** at 99.
2. Periodically toggle the IMPULSE COUNTER to RESET and back to CONT.

SECTION 7

DIAGRAMS

7.1 This section contains functional diagrams, parts location diagrams, and schematic diagrams for the Model 4002 Transmission And Impulse Noise Distribution Set.

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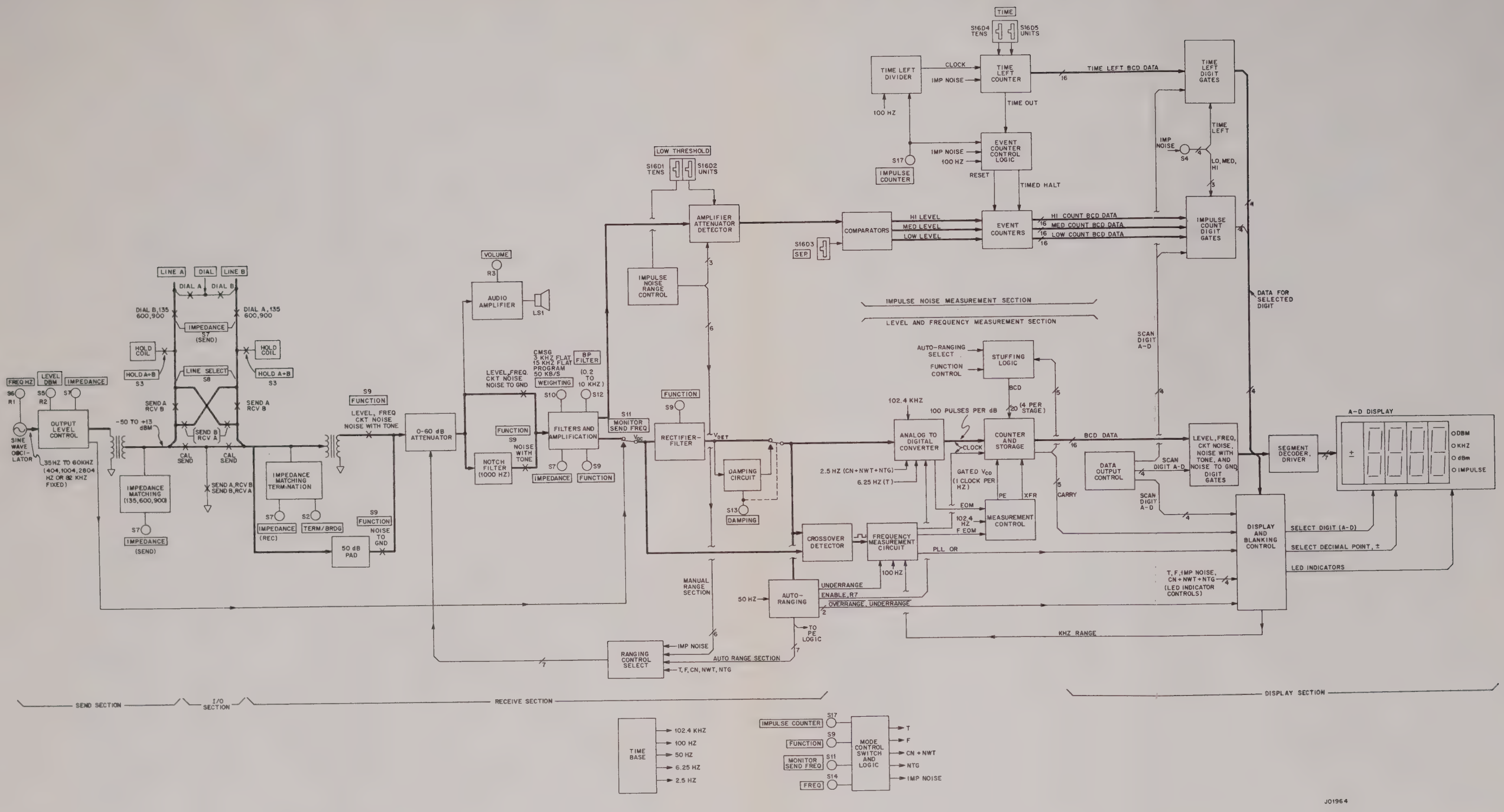


Figure 7—1. Model 4002 General Block Diagram.

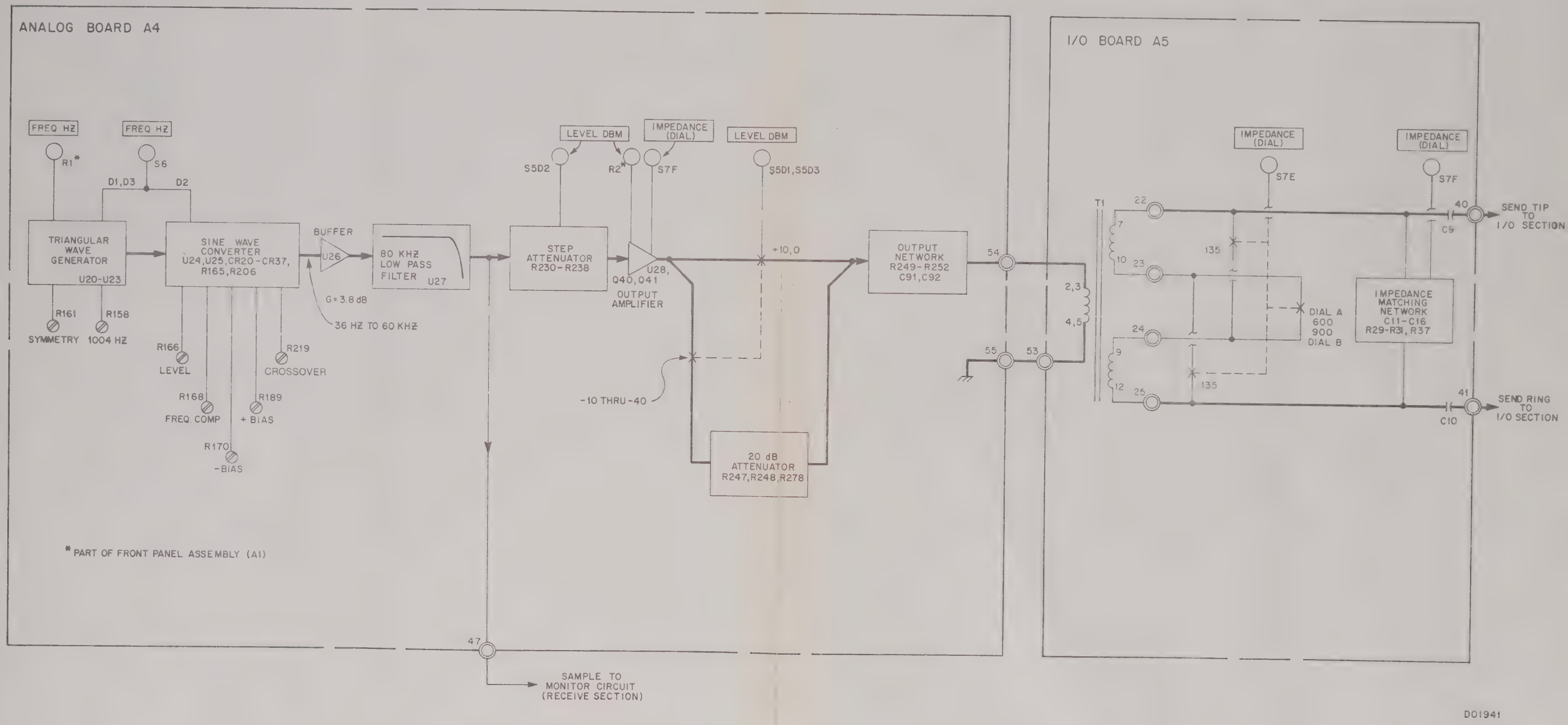


Figure 7—2. Send Section Functional Diagram.

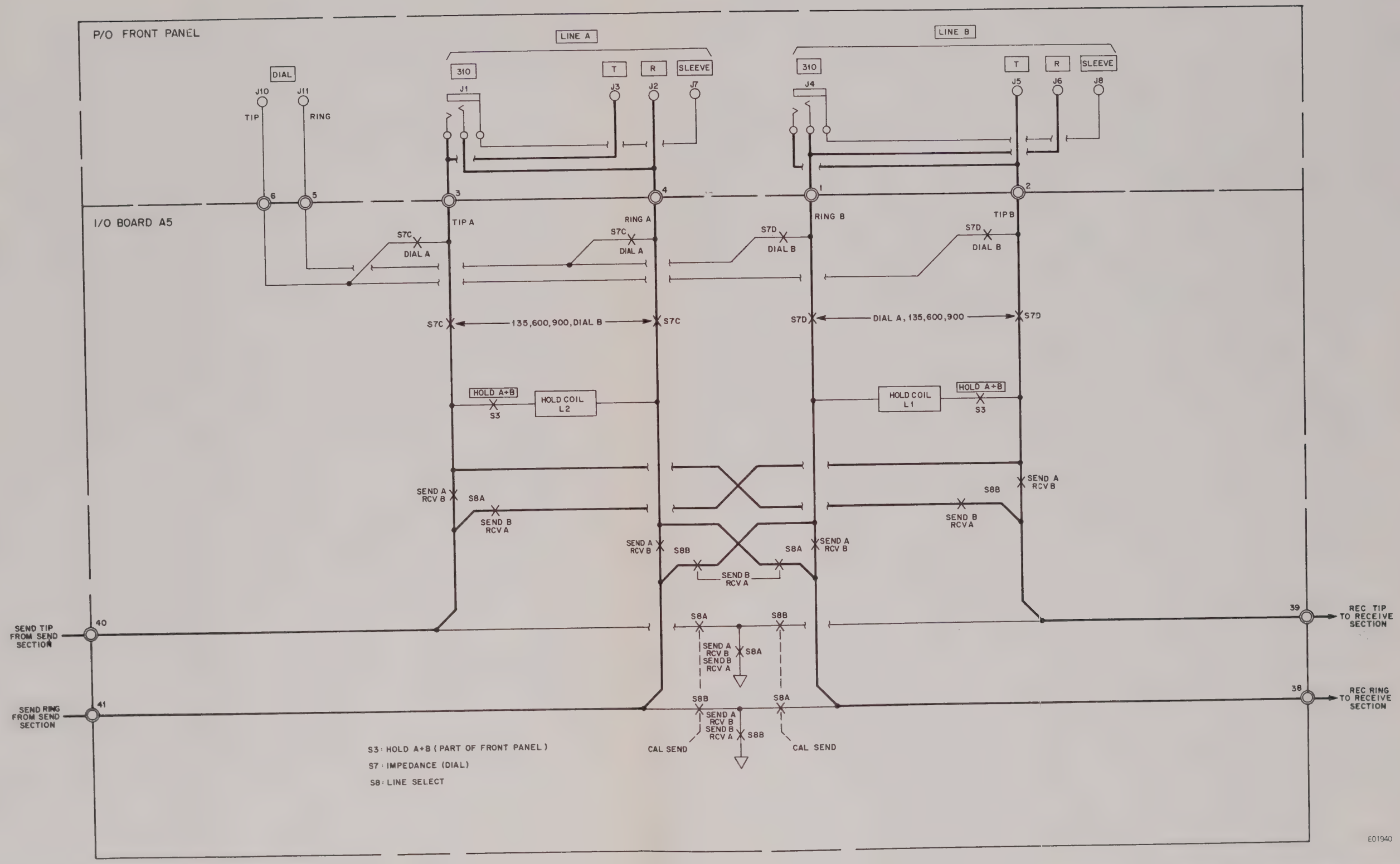


Figure 7—3. Input-Output Section Functional Diagram.

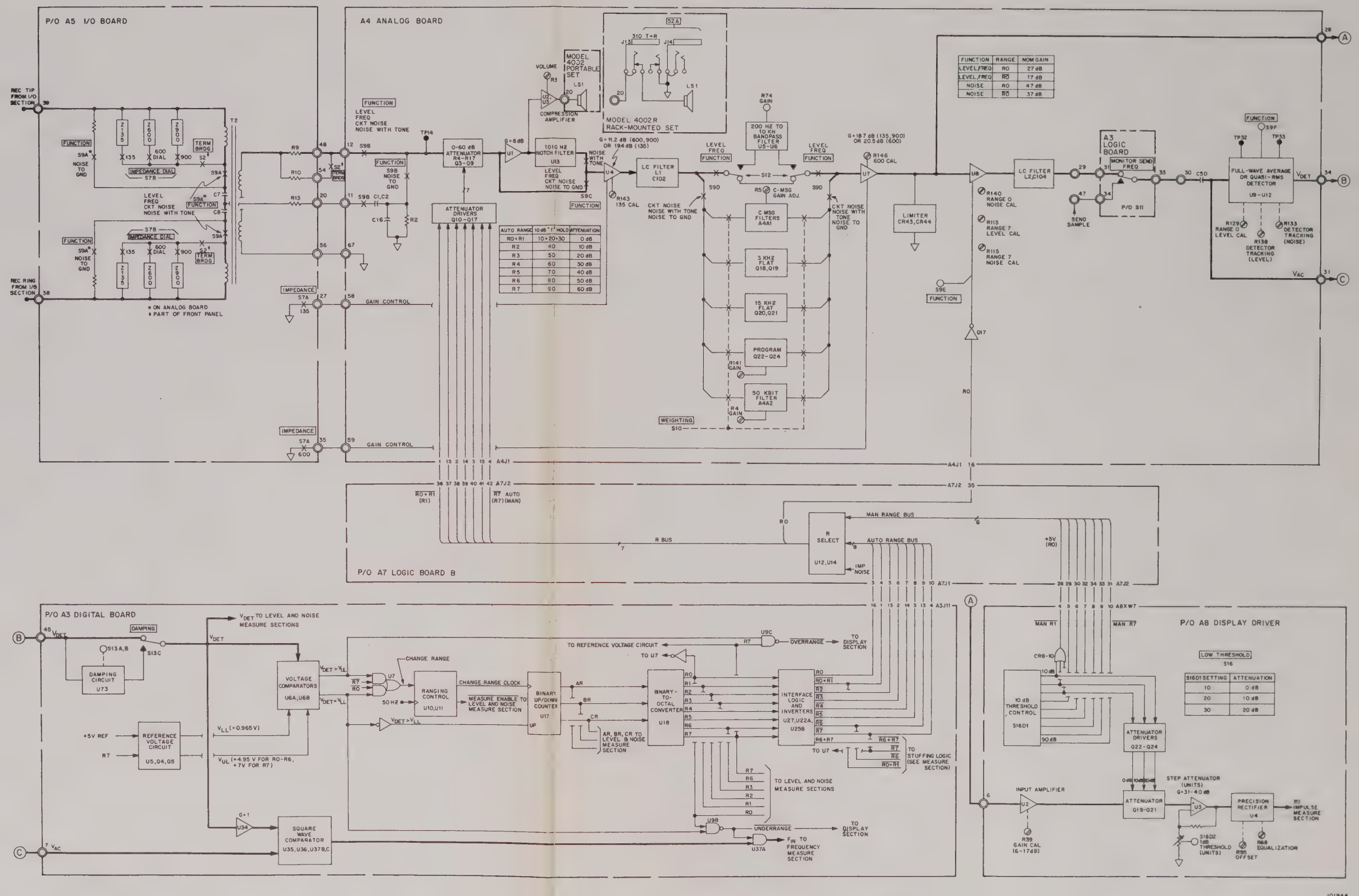


Figure 7—4. Receive Section Functional Diagram.

P/O A3 DIGITAL BOARD

100 HZ
F
FREQUENCY GATE GENERATOR
U43D,U55,U60,U57C,D
FREQ EOM
FREQ GATE
102.4 KHZ
STORE AND STUFF CONTROL U52,U53B
PE
XFR
250 mSEC

PE
DIGIT A COUNTER U38
DIGIT A STORAGE U44
DIGIT B COUNTER U39
DIGIT B STORAGE U45
DIGIT C COUNTER U40
DIGIT C STORAGE U46
DIGIT D COUNTER U41
DIGIT D STORAGE U47
DIGIT E COUNTER U42
UP
$\overline{CO1}$
$\overline{CO2}$
$\overline{CO3}$
$\overline{CO4}$
$\overline{CO5}$
2^0
2^3
TO DISPLAY SECTION

F_{IN} FROM RECEIVE SECTION
PHASE COMPARATOR P/O U32
$\frac{F_{VCO}}{4}$
DIVIDE BY 4 U33
ERROR VOLTAGE
F
VOLTAGE CONTROLLED OSCILLATOR P/O U32
U57A,B
330pF
0.0027
0.018
0.082
0.68
U31A
U31B
U31D
U31C

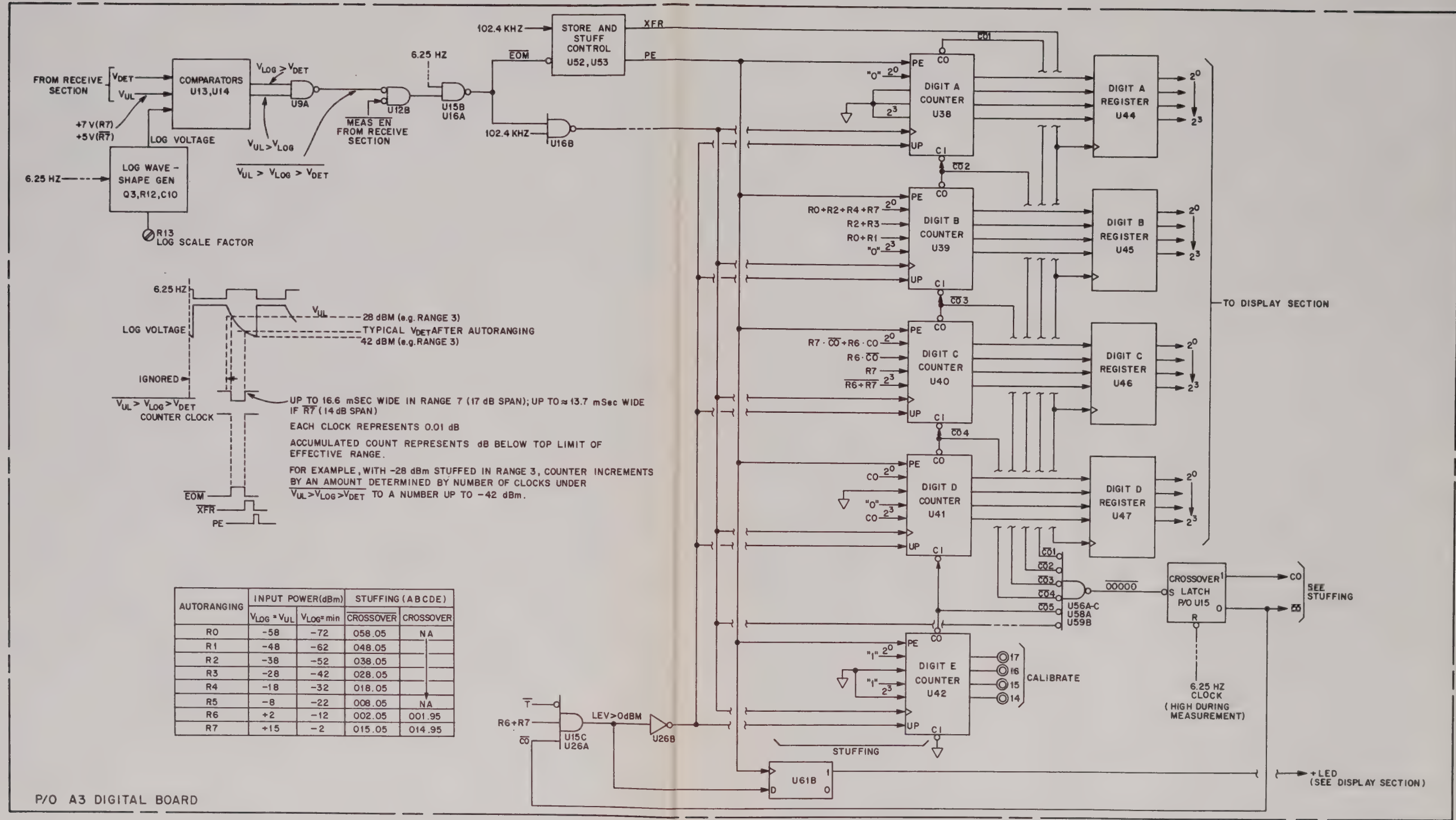
+12V
R40
0.88 V_{DD}
HI LIMIT
R39
0.12 V_{DD}
LO LIMIT
R38
ERROR LIMIT DETECTOR U28,U29A,B
U29D
WRITE 0000
E<MAX
IN LIMIT
100 HZ
BINARY UP/DOWN COUNTER U30
PE
CO
UP/DN
INHIBIT
2^0
2^1
2^2
2^3

U43B
KHZ
U43A,C
DATA STREAM
CALIBRATE
17
16
15
14
PLL OR KHZ
TO DISPLAY SECTION

A3XA15
7
A3J12-5
A7J1-44
P/O A7 LOGIC BOARD B
A3J12
8 — 50 $\overline{CO1}$
7 — 48 $\overline{CO2}$
13 — 41 DATA STREAM
A7J1
AUTOMATIC RANGE CONTROL U4,U5,U7,U8
A7J1
32 KHZ

D01978

Figure 7—5. Frequency Measurement Functional Diagram.



AUTORANGING	INPUT POWER(dBm)		STUFFING (ABCDE)	
	$V_{LOG} = V_{UL}$	V_{LOG} = min	$\overline{\text{CROSSOVER}}$	CROSSOVER
R0	-58	-72	058.05	NA
R1	-48	-62	048.05	
R2	-38	-52	038.05	
R3	-28	-42	028.05	
R4	-18	-32	018.05	
R5	-8	-22	008.05	NA
R6	+2	-12	002.05	001.95
R7	+15	-2	015.05	014.95

D01977

Figure 7—6. Tone Level Measurement Functional Diagram.

AUTO-RANGING	CKT NOISE & NOISE WITH TONE (dBrn)		NOISE TO GND (dBrn)		CKT NOISE & NOISE WITH TONE STUFFING	NOISE TO GND STUFFING
	$V_{LOG} = V_{UL}$	$V_{LOG} = V_{LL}$	$V_{LOG} = V_{UL}$	$V_{LOG} = V_{LL}$		
R0	12	0	62	48	012.50	062.50
R1	22	8	72	58	022.50	072.50
R2	32	18	82	68	032.50	082.50
R3	42	28	92	78	042.50	092.50
R4	52	38	102	88	052.50	102.50
R5	62	48	112	98	062.50	112.50
R6	72	58	122	108	072.50	122.50
R7	85	68	135	118	085.50	135.50

D01979

Figure 7—7. Noise Measurement Functional Diagram.

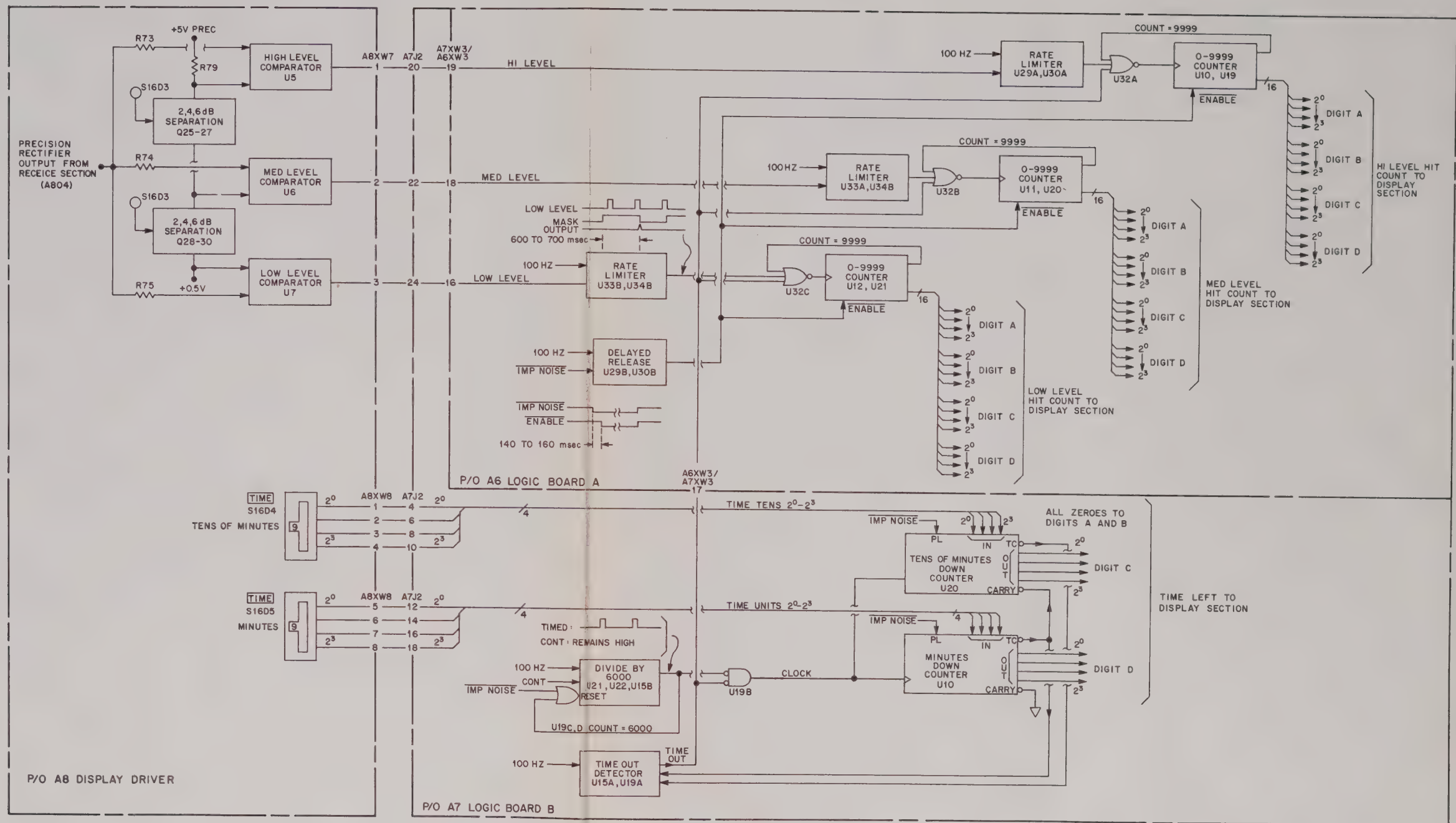


Figure 7—8. Impulse Noise Measurement Functional Diagram.

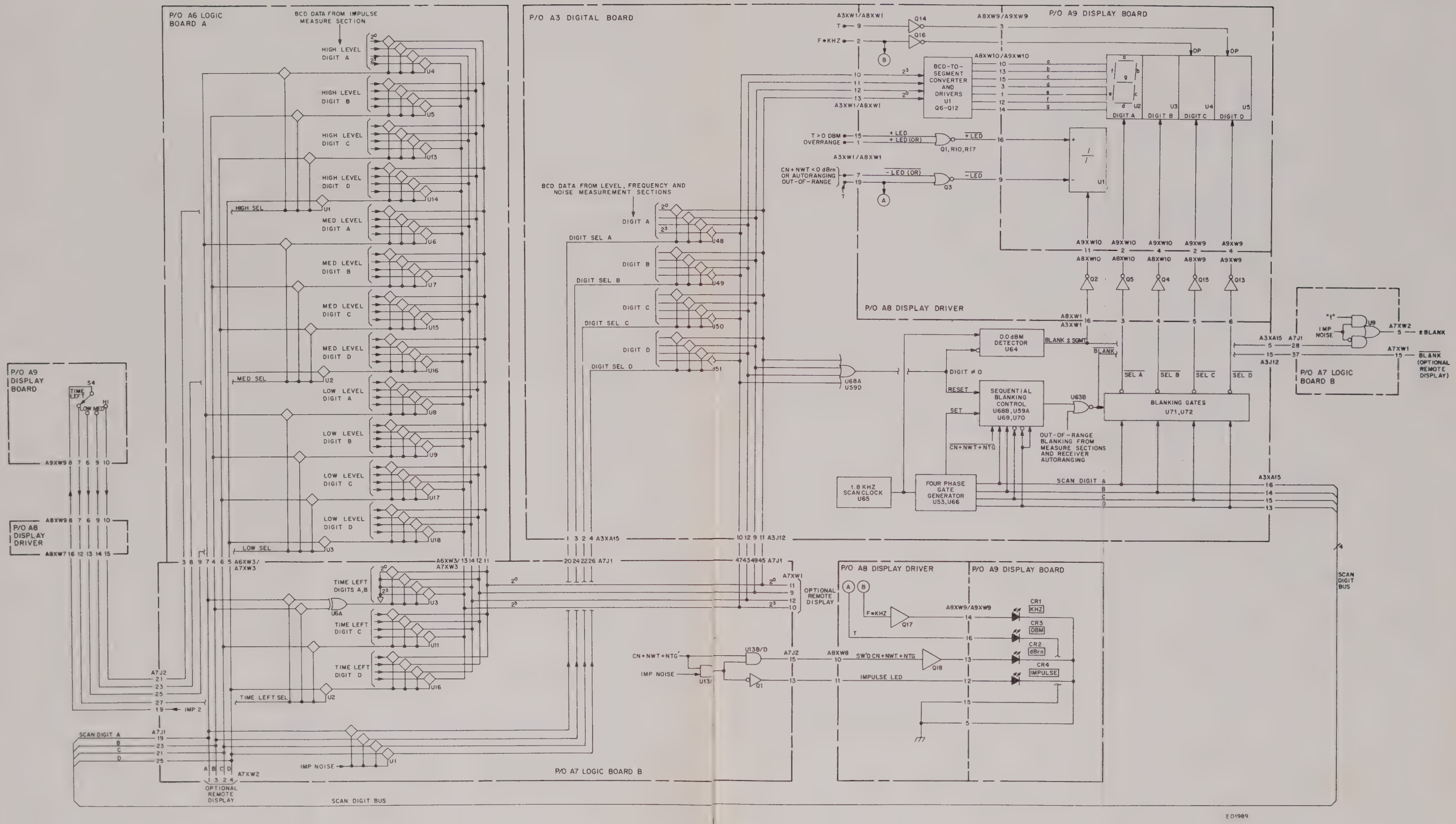


Figure 7—9. Display Section Functional Diagram.

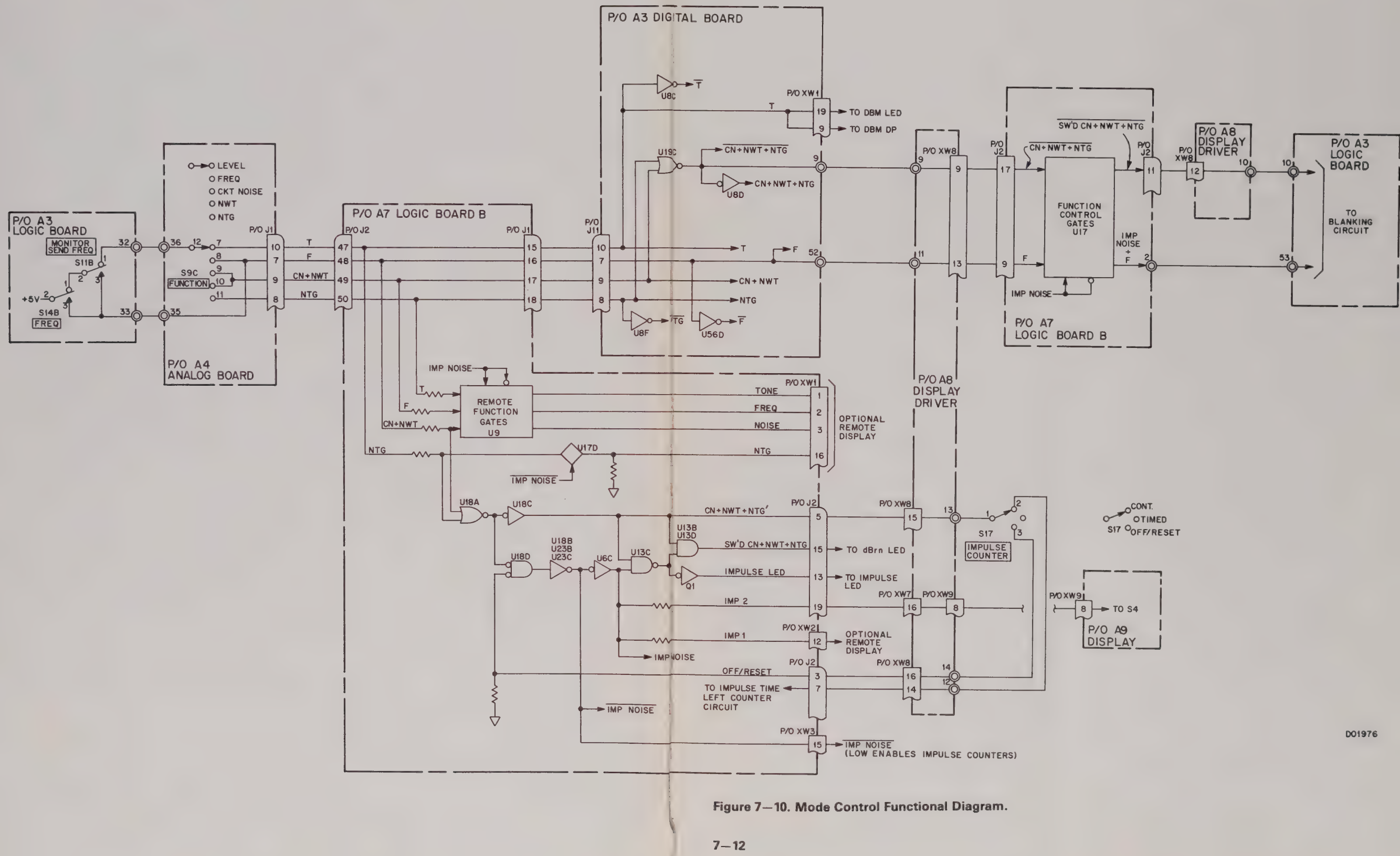
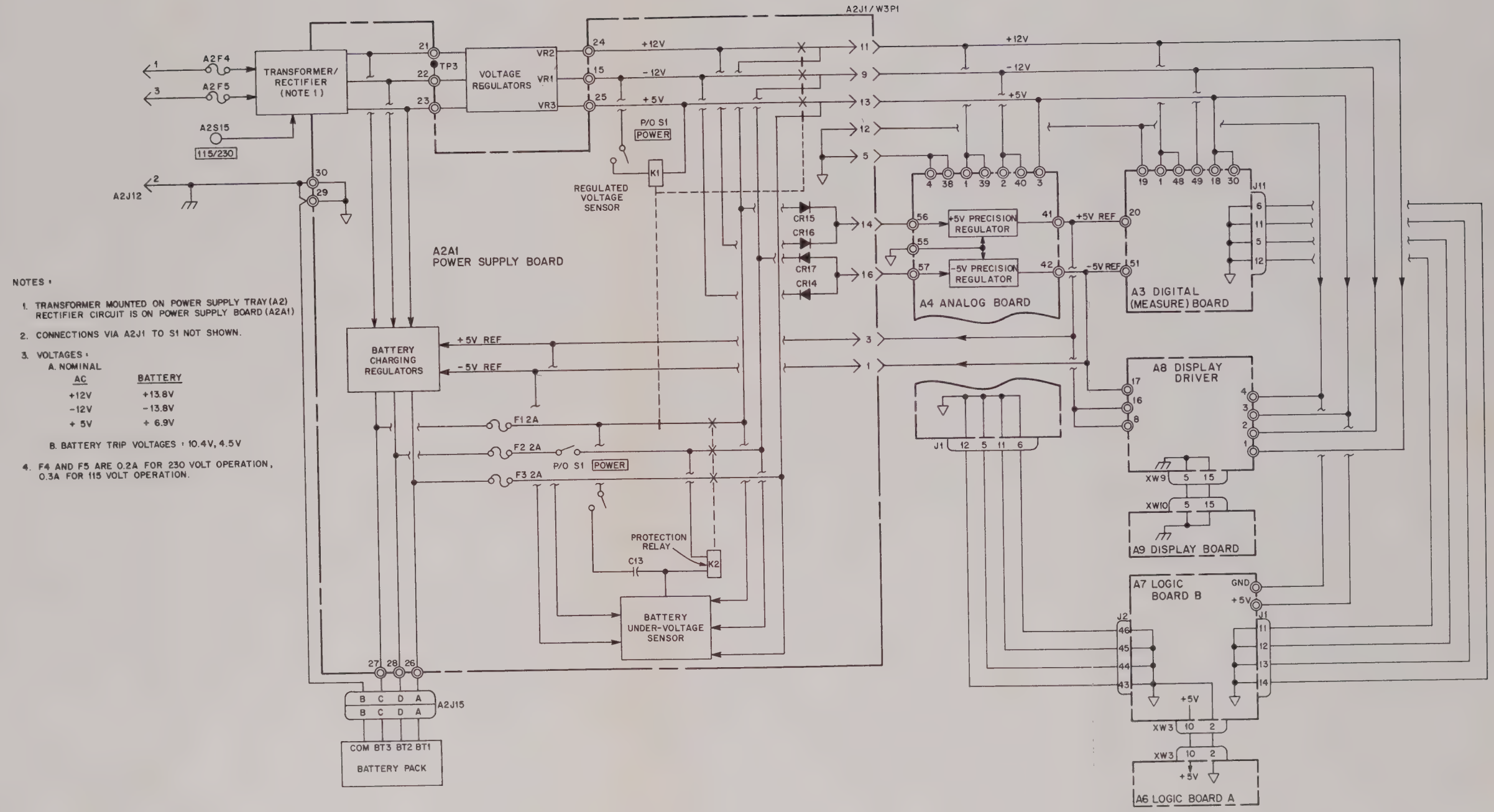


Figure 7—10. Mode Control Functional Diagram.



D01987

Figure 7—11. Power Supply and Distribution Functional Diagram.

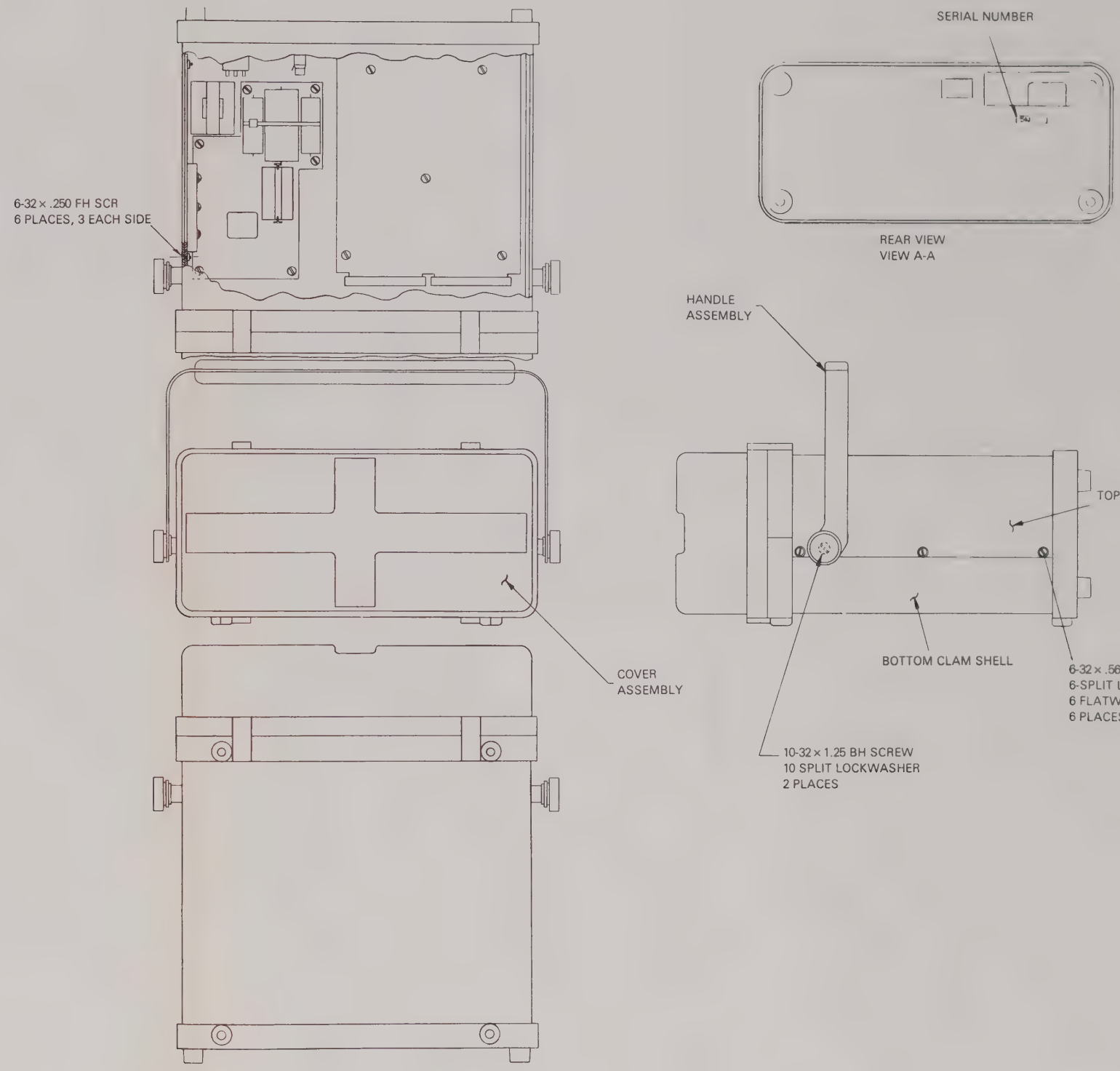
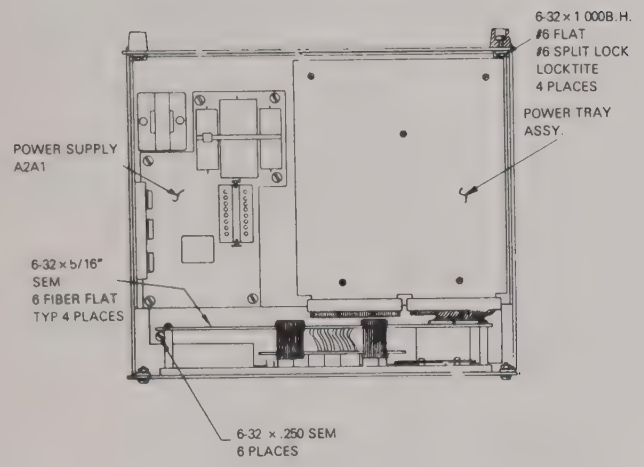
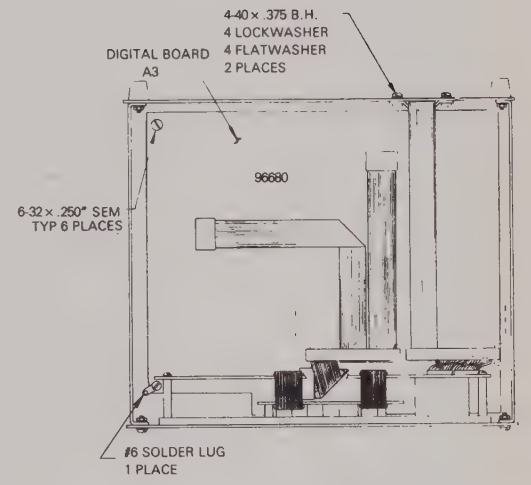
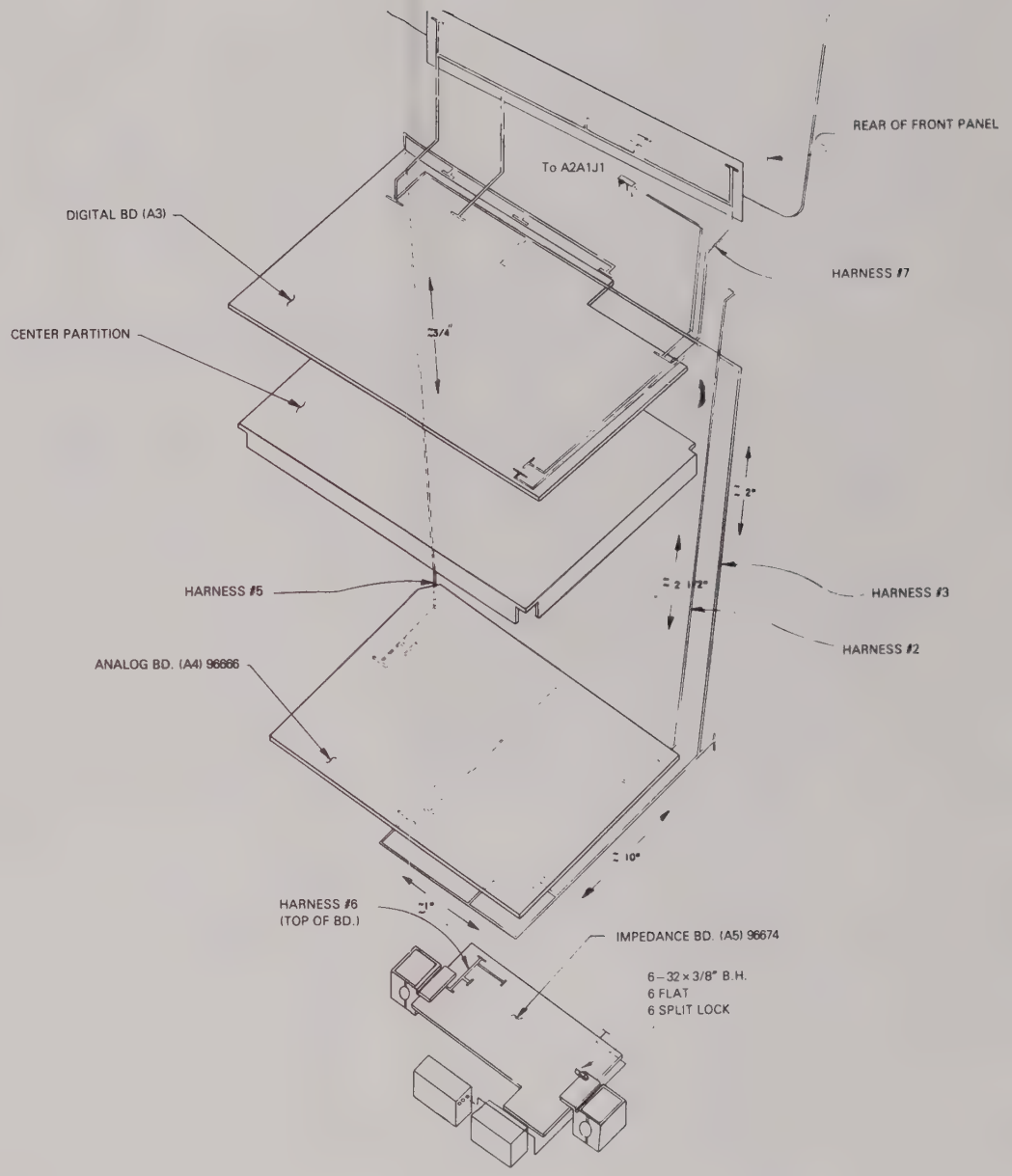
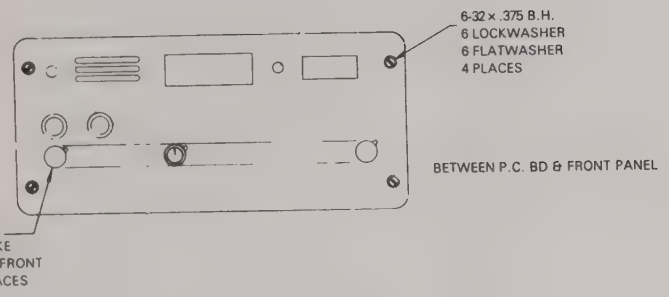


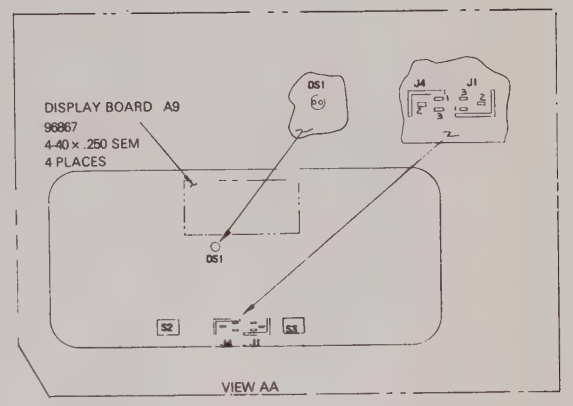
Figure 7—12. Model 4002 Top Unit Assembly Diagram.

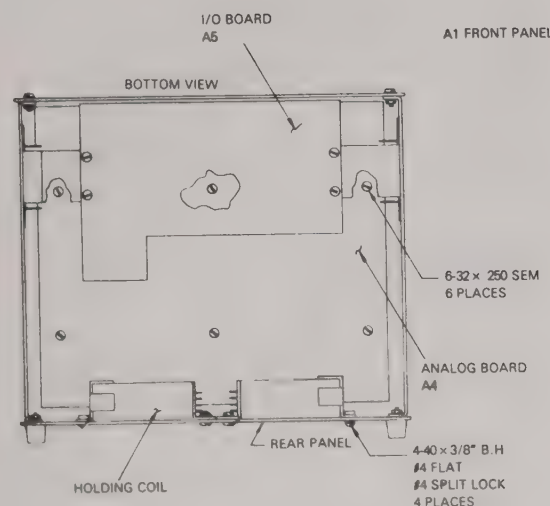












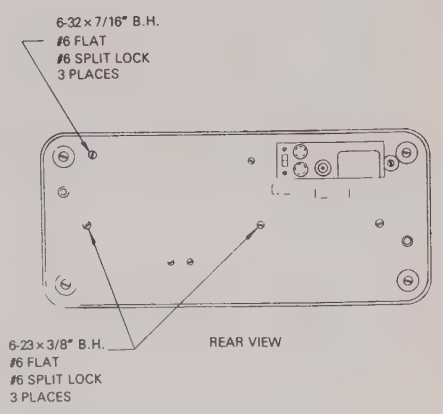


Figure 7—13. Model 4002 Overall Assembly Diagram.

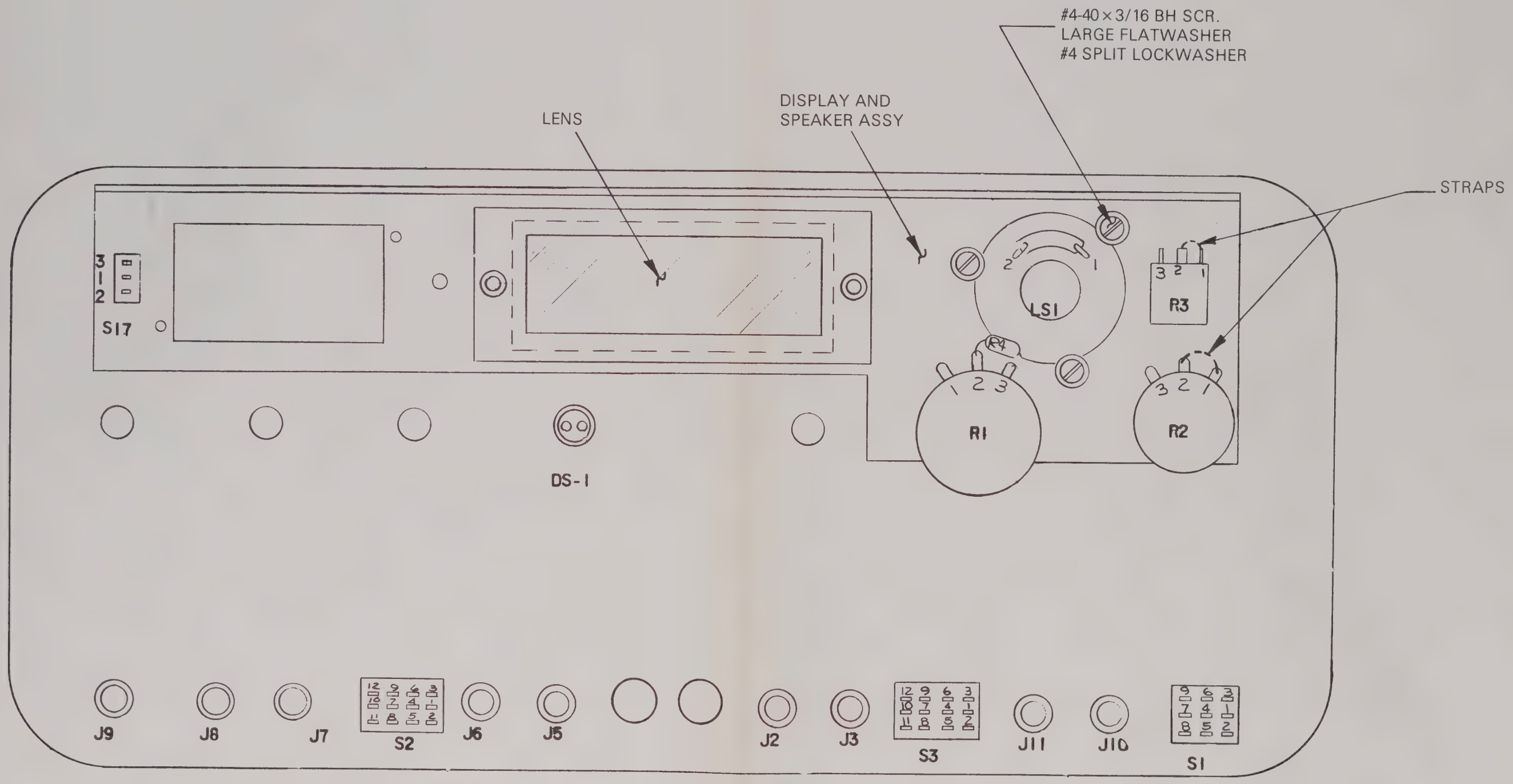
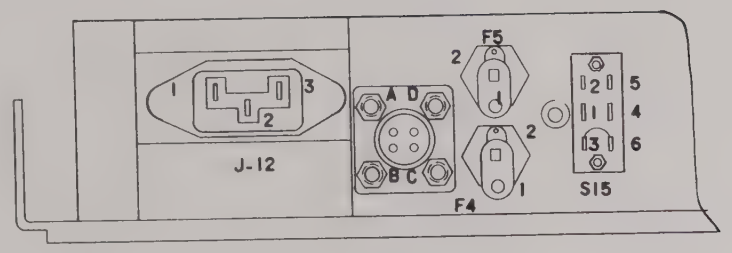
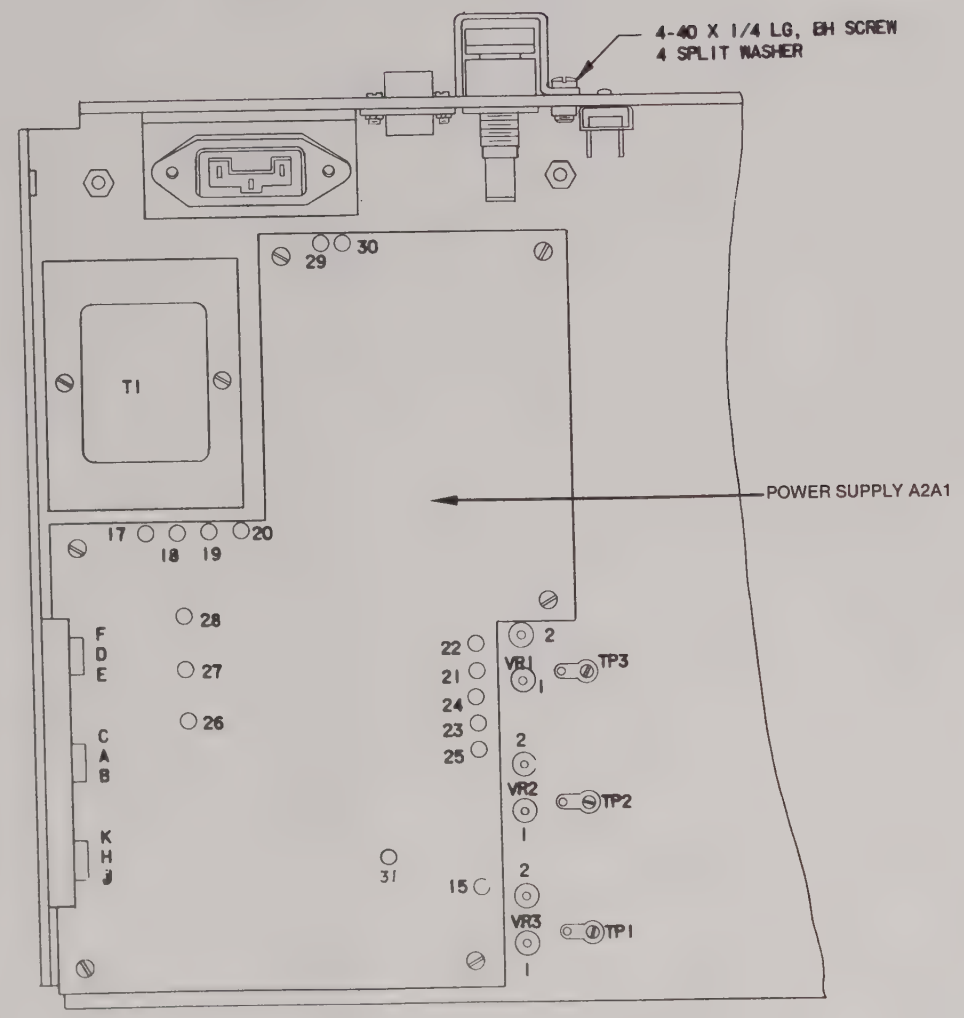


Figure 7—14. Front Panel Assembly Diagram.

SECTION A-A





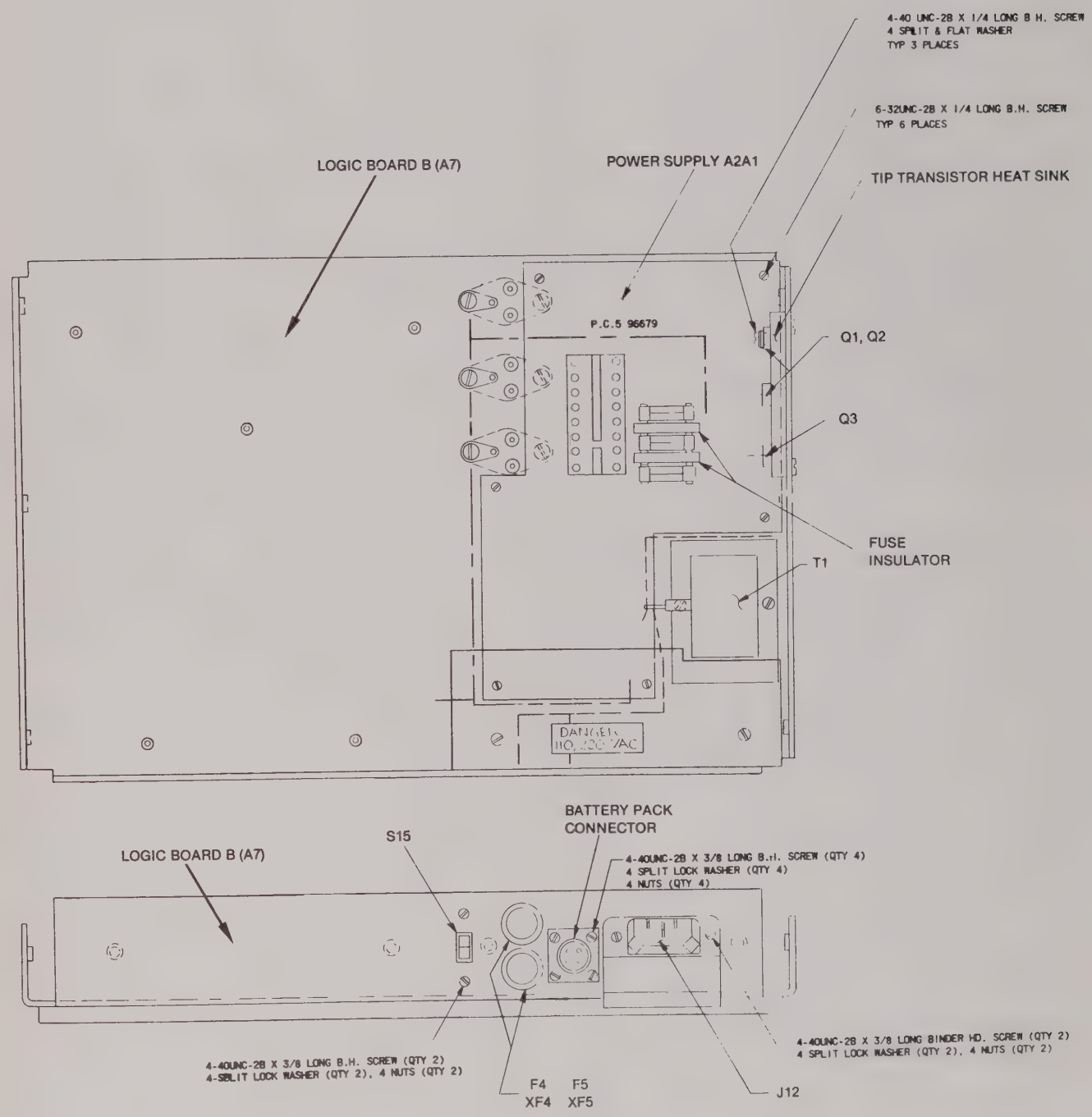
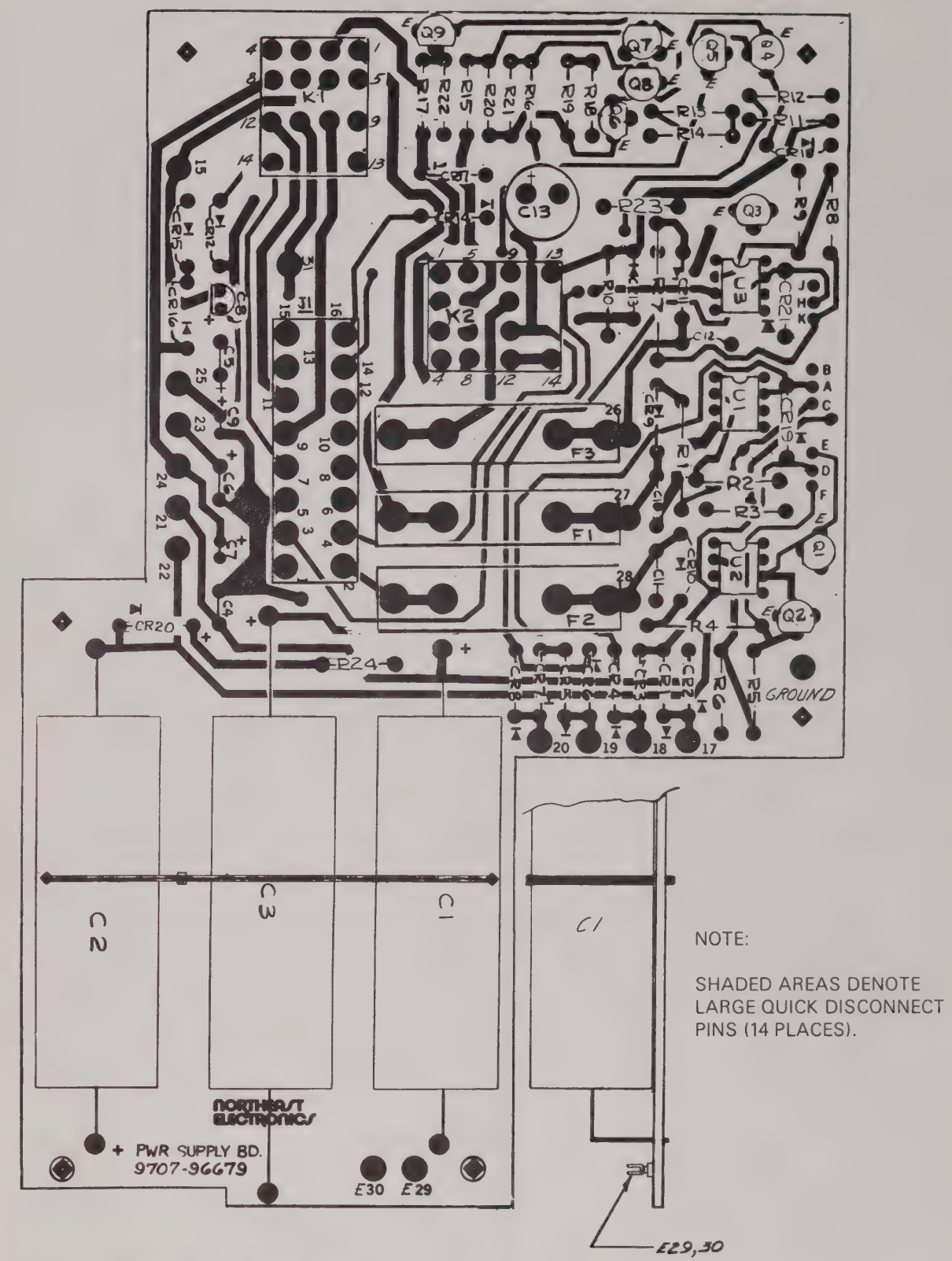


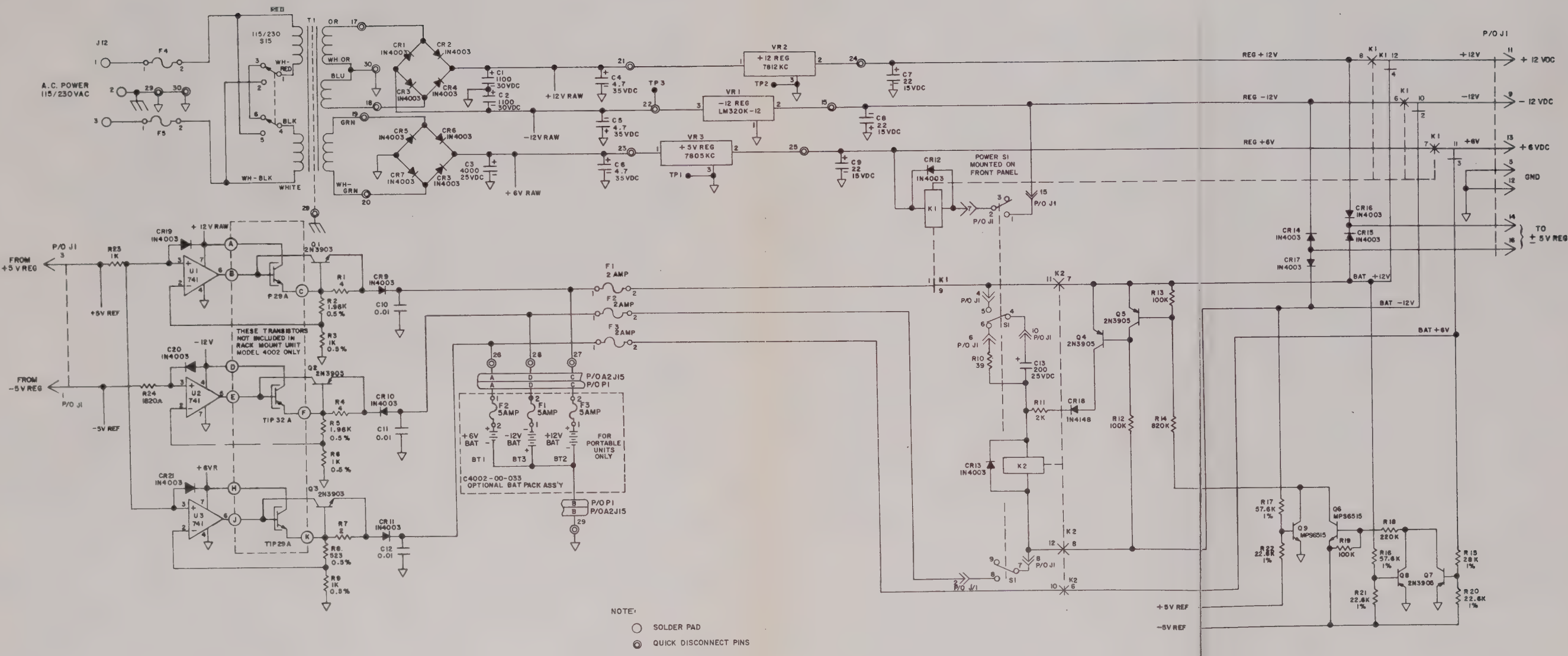
Figure 7—15. Power Supply Assembly Diagram.



NOTE:

SHADED AREAS DENOTE LARGE QUICK DISCONNECT PINS (14 PLACES).

Figure 7—16. Power Supply Board Parts Location Diagram.



NOTE:

○ SOLDER PAD

◎ QUICK DISCONNECT PINS

POWER SUPPLY	
NE PART NO.	C0044-00-025
REF DESIG	A2A1
PC NO.	96679

Figure 7—17. Power Supply Schematic Diagram.

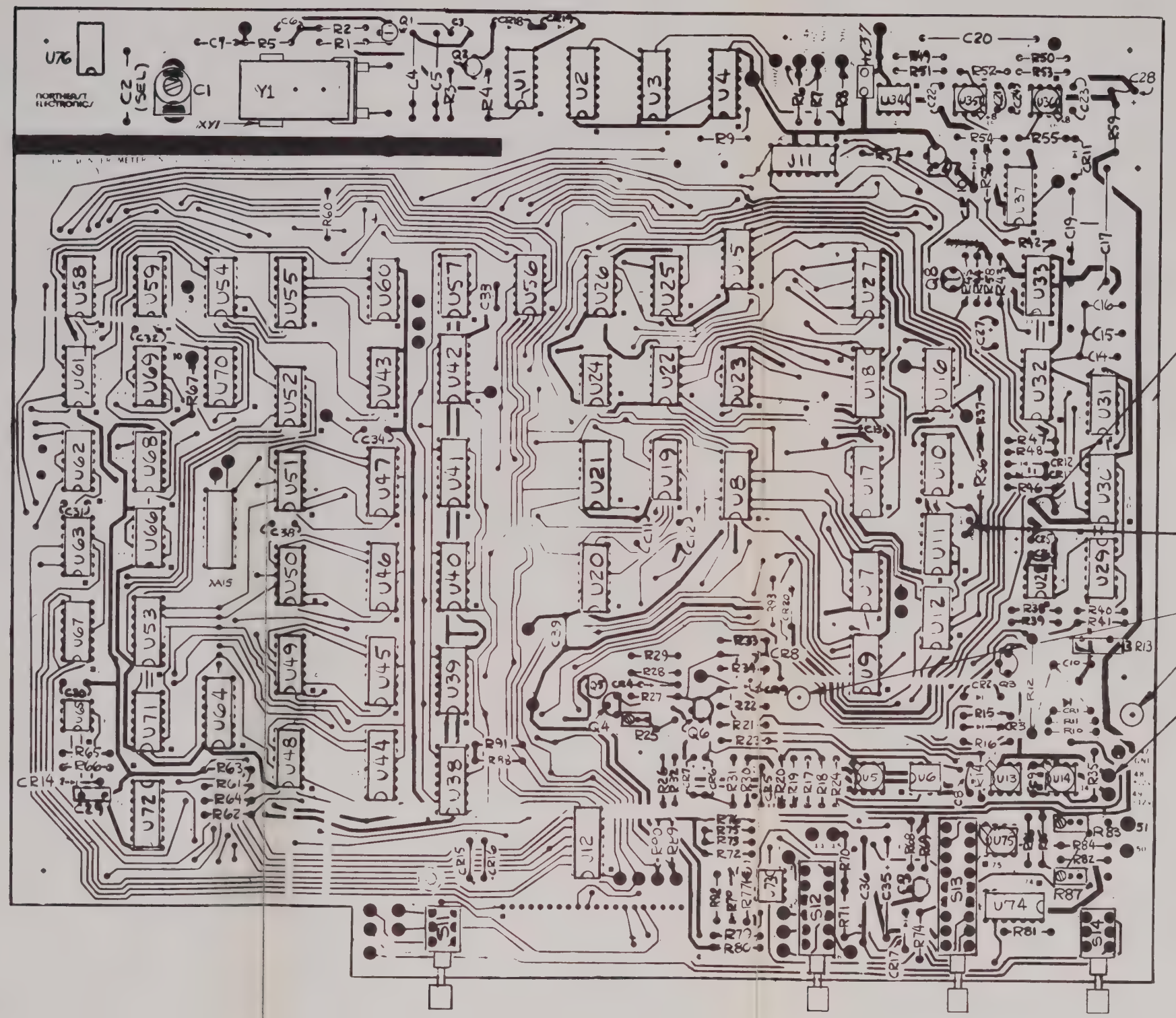

STRAP 26 TO 27 IF U30 IS CD4029AE
27 TO 28 IF U30 IS MC14510
STRAP 23 TO 25
7/16 x 4-40 SWDG STANDOFF
COMPONENT SIDE
SEE NOTE 1
NOTES:
1. ● DENOTES LARGE QUICK DISCONNECTS LOCATED ON SIDE SHOWN TYPICAL 45 PLACES.

Figure 7—18. Digital Board Parts Location Diagram.

DAMPING CIRCUIT

LEVEL NOISE LOGGER

LIMIT COMPARATOR AND RANGE SELECTOR

PHASE LOCKED LOOP AND 4 x MULTIPLIER

DIGITAL BOARD	
NE PART NO.	C4002-00-025
REF DESIG	A3
PC NO.	96680

Figure 7—19. Digital Board Schematic Diagram. (Sheet 1 of 3)

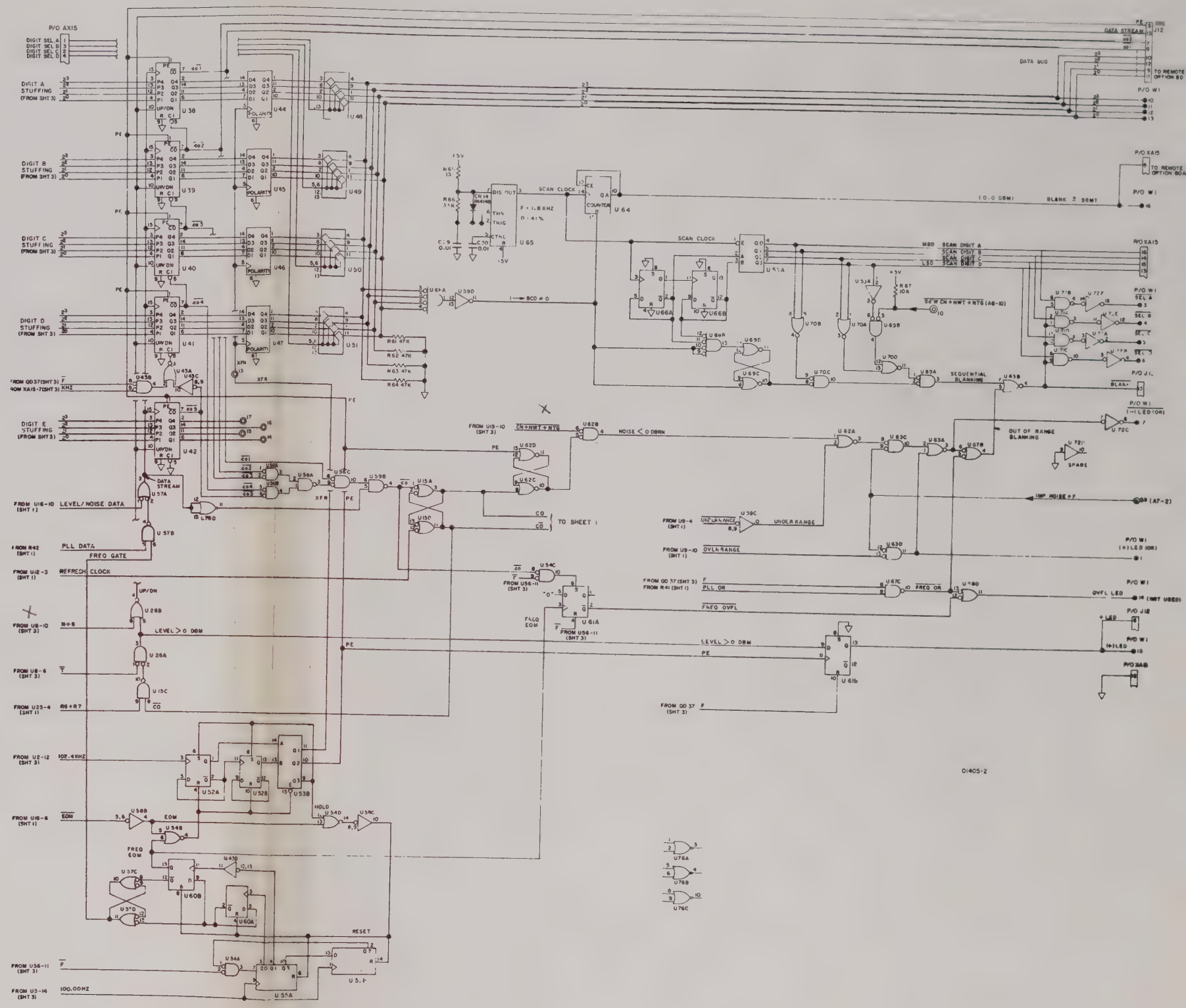


Figure 7—19. Digital Board Schematic Diagram. (Sheet 2 of 3)

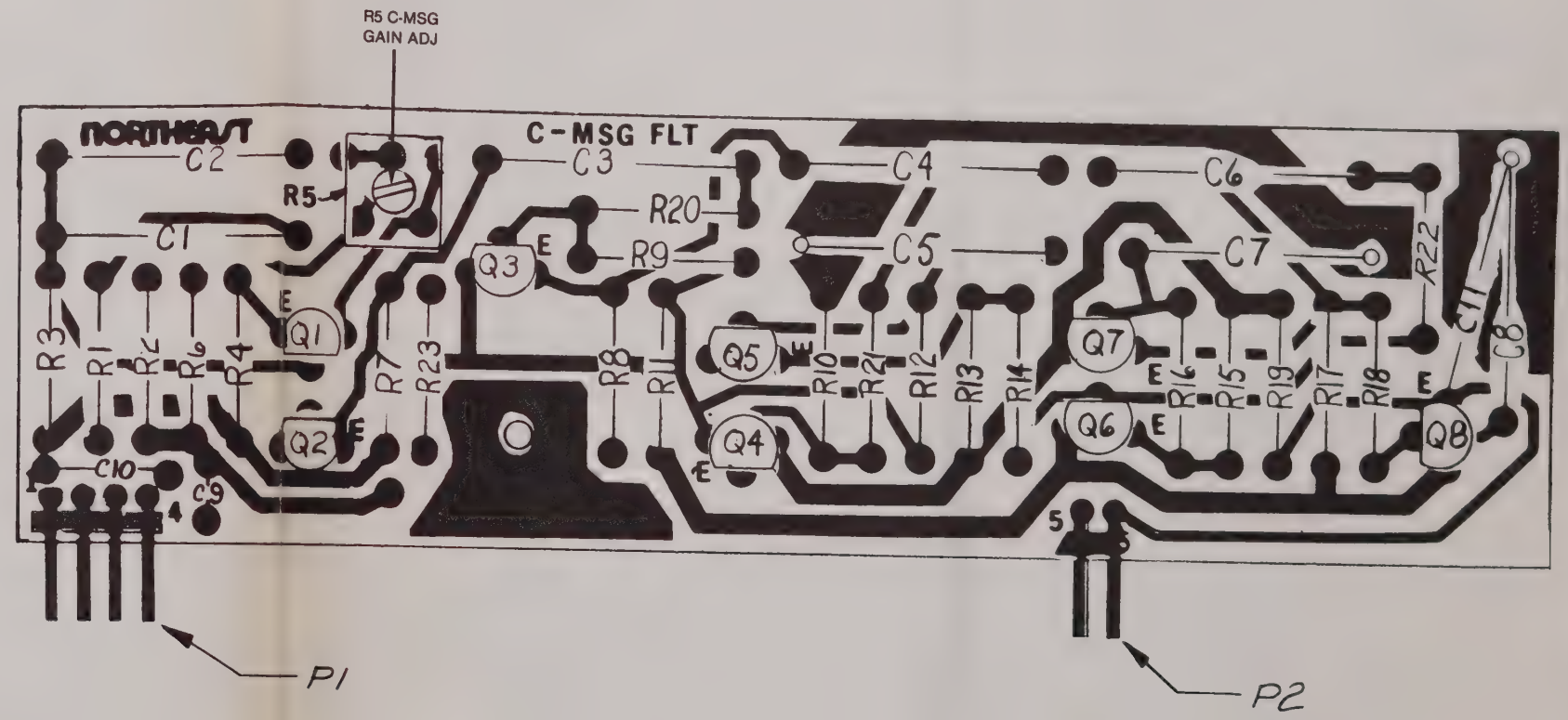
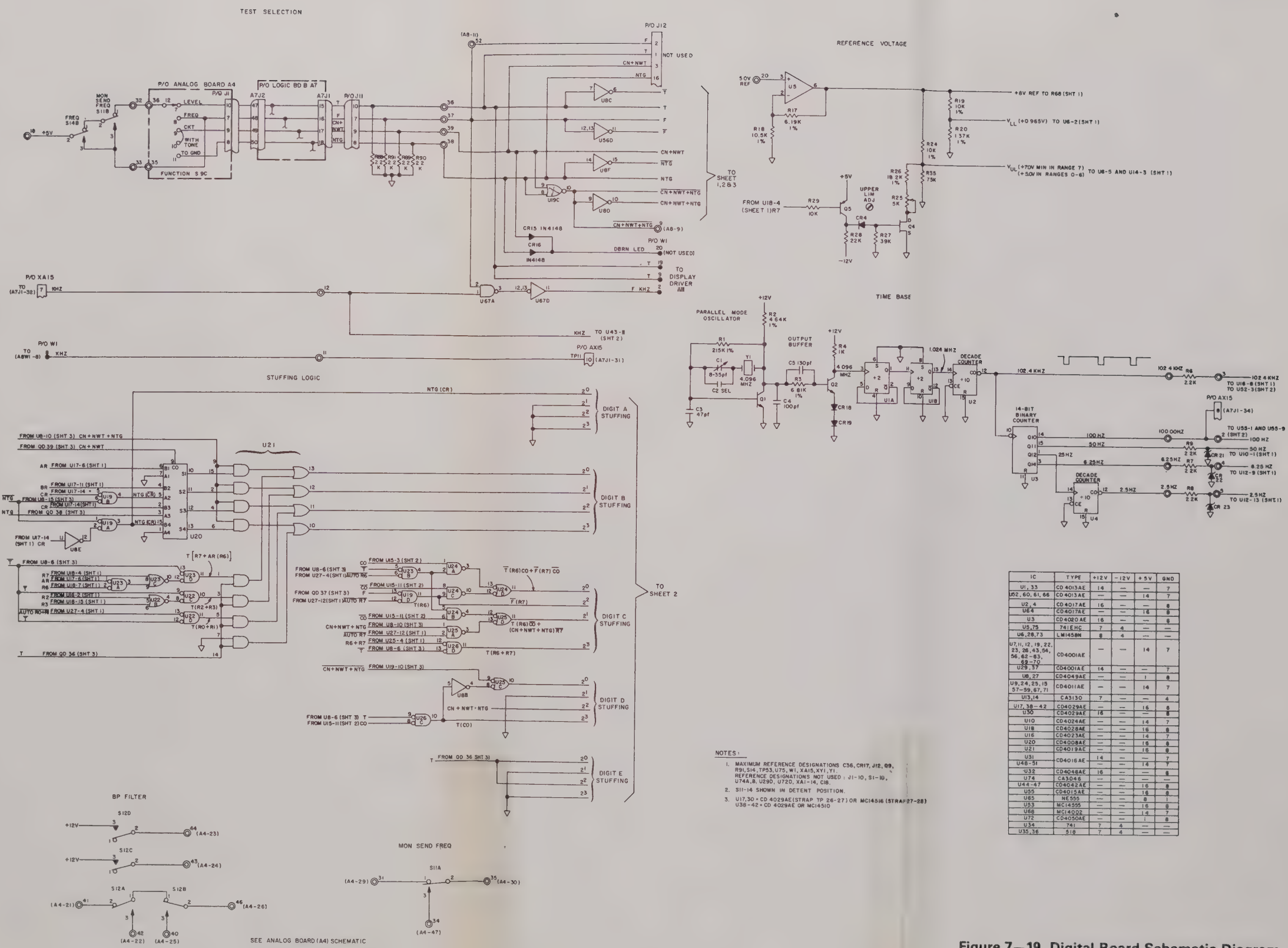


Figure 7—20. C-Message Filter Board Parts Location Diagram.



NOTES:

1. MAXIMUM REFERENCE DESIGNATIONS C36, CR17, J12, S9, R91, S14, TP53, U75, W1, XA15, XY1, Y1. REFERENCE DESIGNATIONS NOT USED: J1-10, S1-10, U74A, B, U290, U720, XA1-14, C18.
2. S11-14 SHOWN IN DETENT POSITION.
3. U17, 30 = CD 4029AE (STRAP TP 26-27) OR MC14516 (STRAP 27-28) U38-42 = CD 4029AE OR MC14510

IC	TYPE	+12V	-12V	+5V	GND
U1, 33	CD 4013AE	14	—	—	7
U52, 60, 61, 66	CD 4013AE	—	—	14	7
U2, 4	CD 4017AE	16	—	—	8
U64	CD 4017AE	—	—	16	8
U3	CD 4020 AE	16	—	—	8
U5, 75	741 EHC	7	4	—	—
U6, 28, 73	LM1458N	8	4	—	—
U7, 11, 12, 19, 22, 23, 26, 43, 54, 56, 62-65, 69-70	CD4001AE	—	—	14	7
U29, 37	CD4001AE	14	—	—	7
U8, 27	CD4049AE	—	—	1	8
U9, 24, 25, 15 57-59, 67, 71	CD4011AE	—	—	14	7
U13, 14	CA3130	7	—	—	4
U17, 38-42	CD4029AE	—	—	16	8
U30	CD4029AE	16	—	—	8
U10	CD4024AE	—	—	14	7
U18	CD4028AE	—	—	16	8
U16	CD4023AE	—	—	14	7
U20	CD4008AE	—	—	16	8
U21	CD4019AE	—	—	16	8
U31	CD4016AE	14	—	—	7
U46-51		—	—	14	7
U32	CD4046AE	16	—	—	8
U74	CA3046	—	—	—	—
U44-47	CD4042AE	—	—	16	8
U35	CD4015AE	—	—	16	8
U65	NE555	—	—	8	1
U53	MC14555	—	—	16	8
U68	MC14002	—	—	14	7
U72	CD4050AE	—	—	1	8
U34	741	7	4	—	—
U35, 36	510	7	4	—	—

Figure 7—19. Digital Board Schematic Diagram. (Sheet 3 of 3)

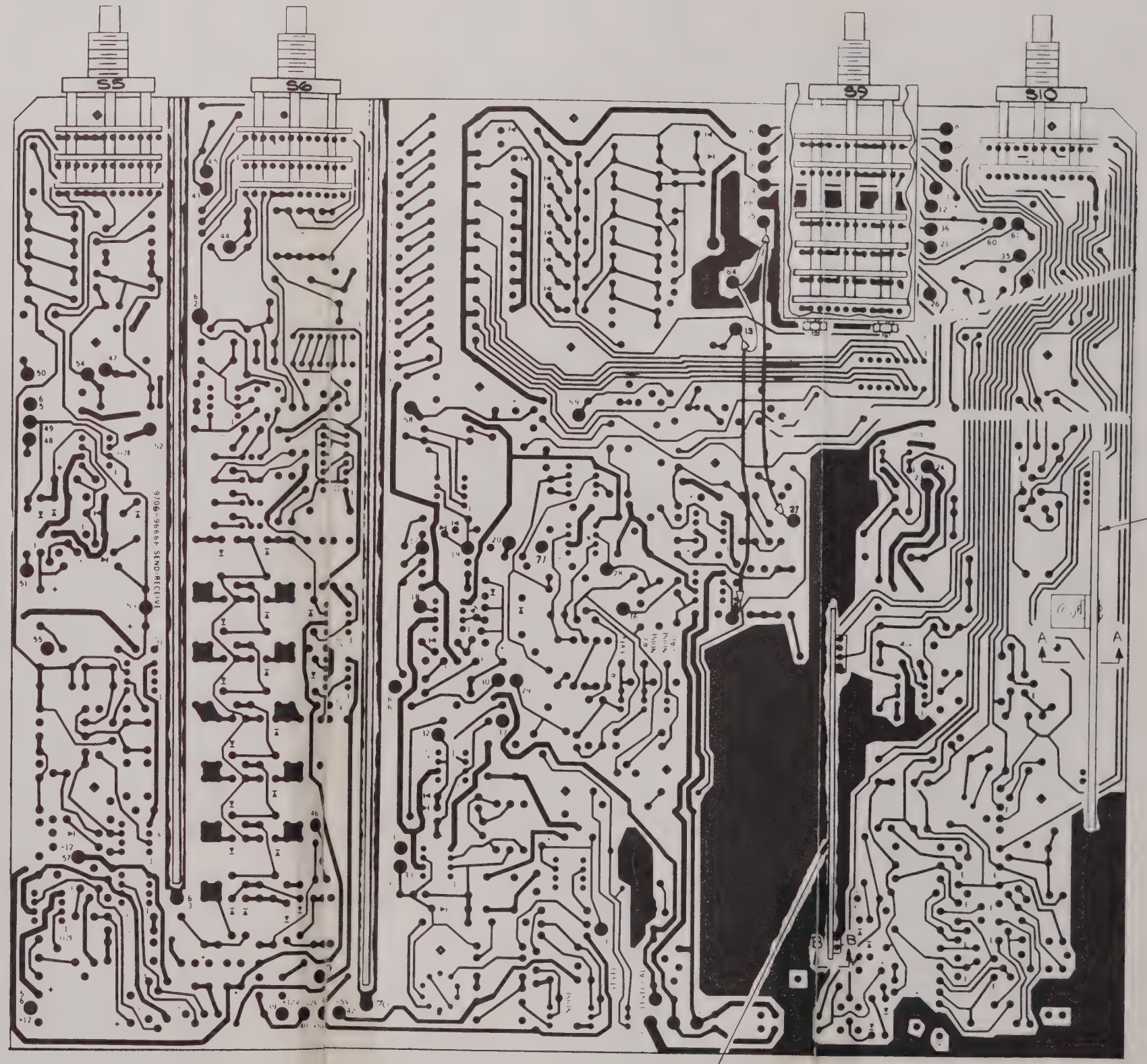


Figure 7—21. Analog Board Parts Location Diagram. (Sheet 1 of 2)

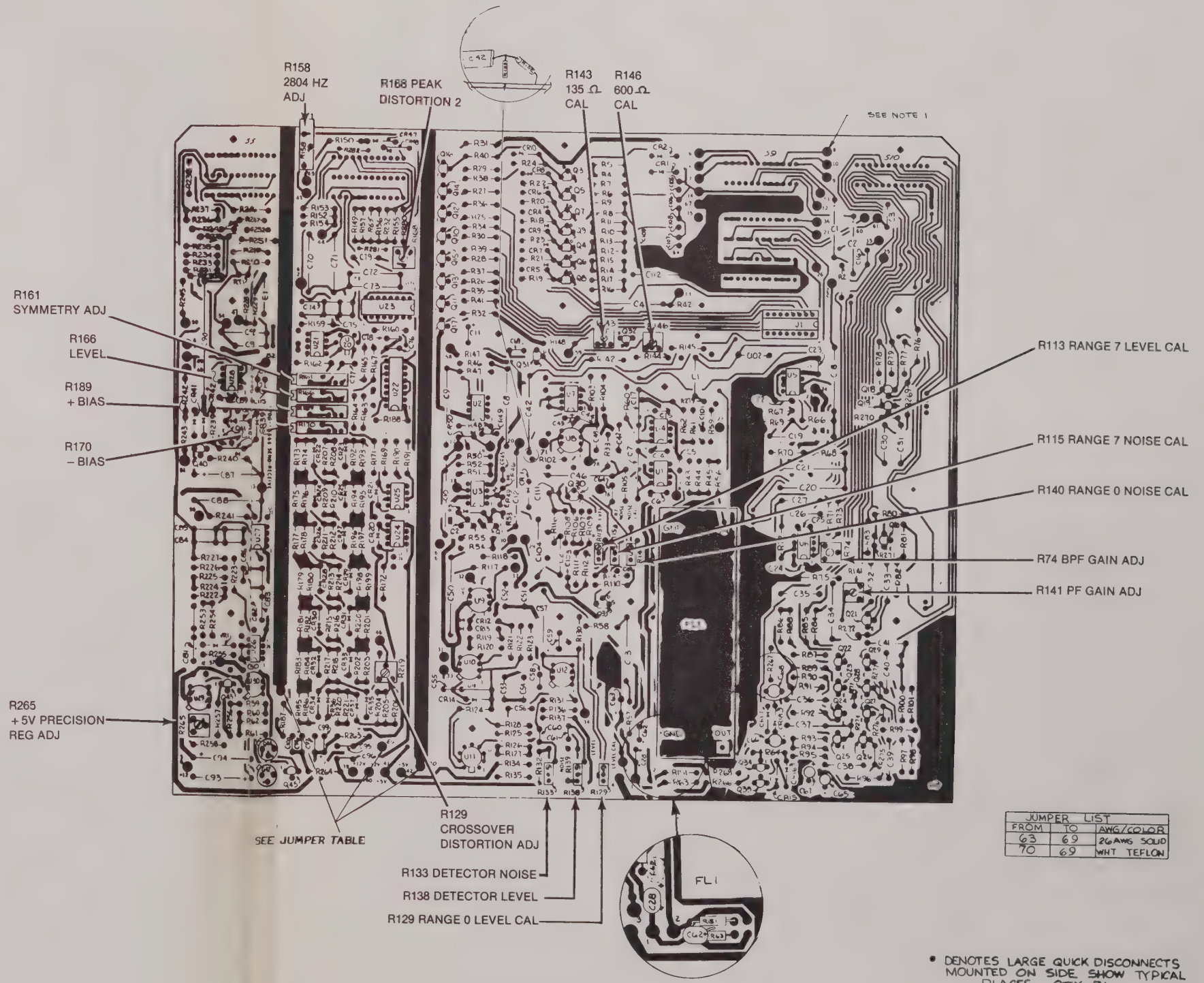
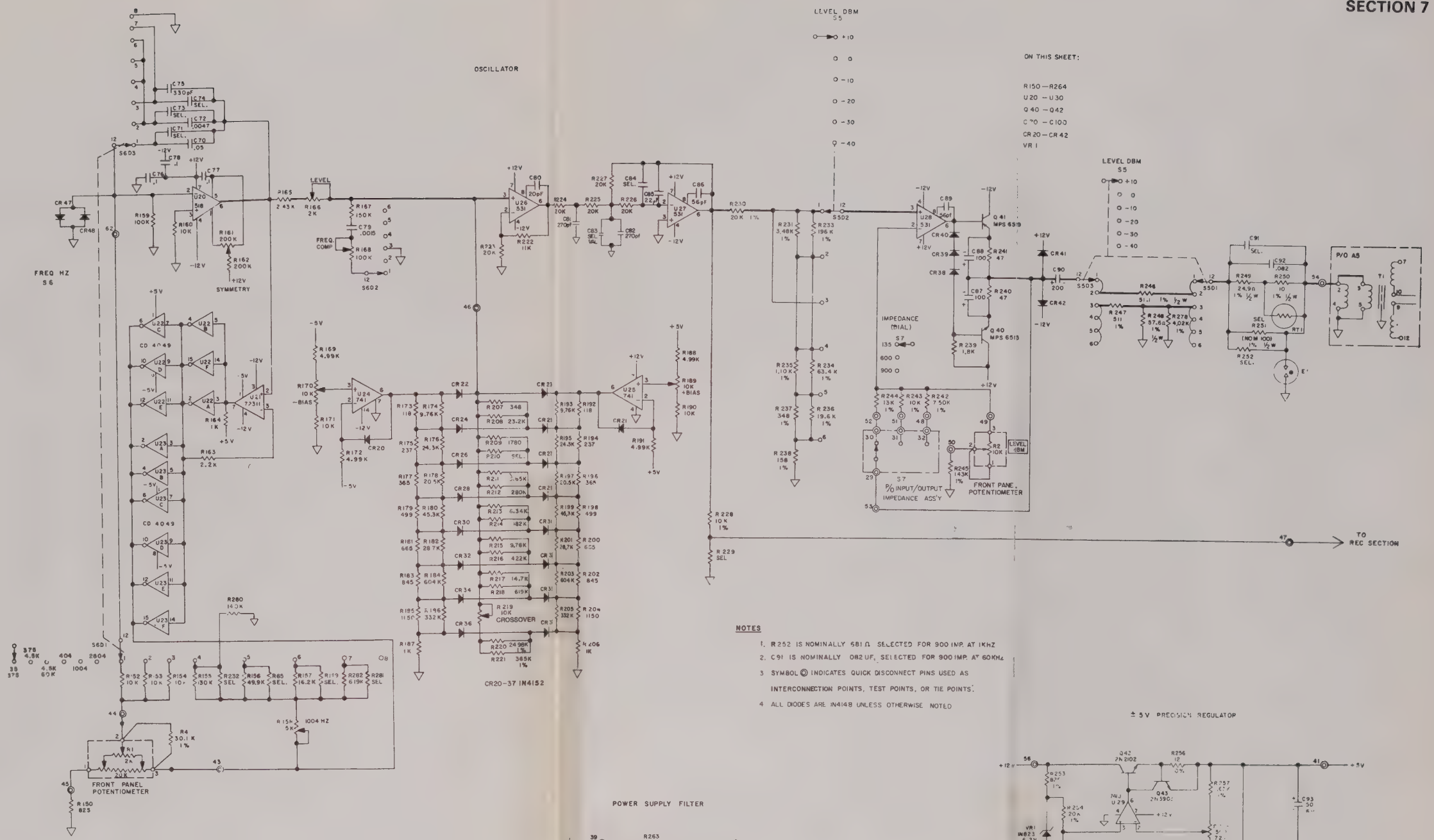


Figure 7—21. Analog Board Parts Location Diagram. (Sheet 2 of 2)



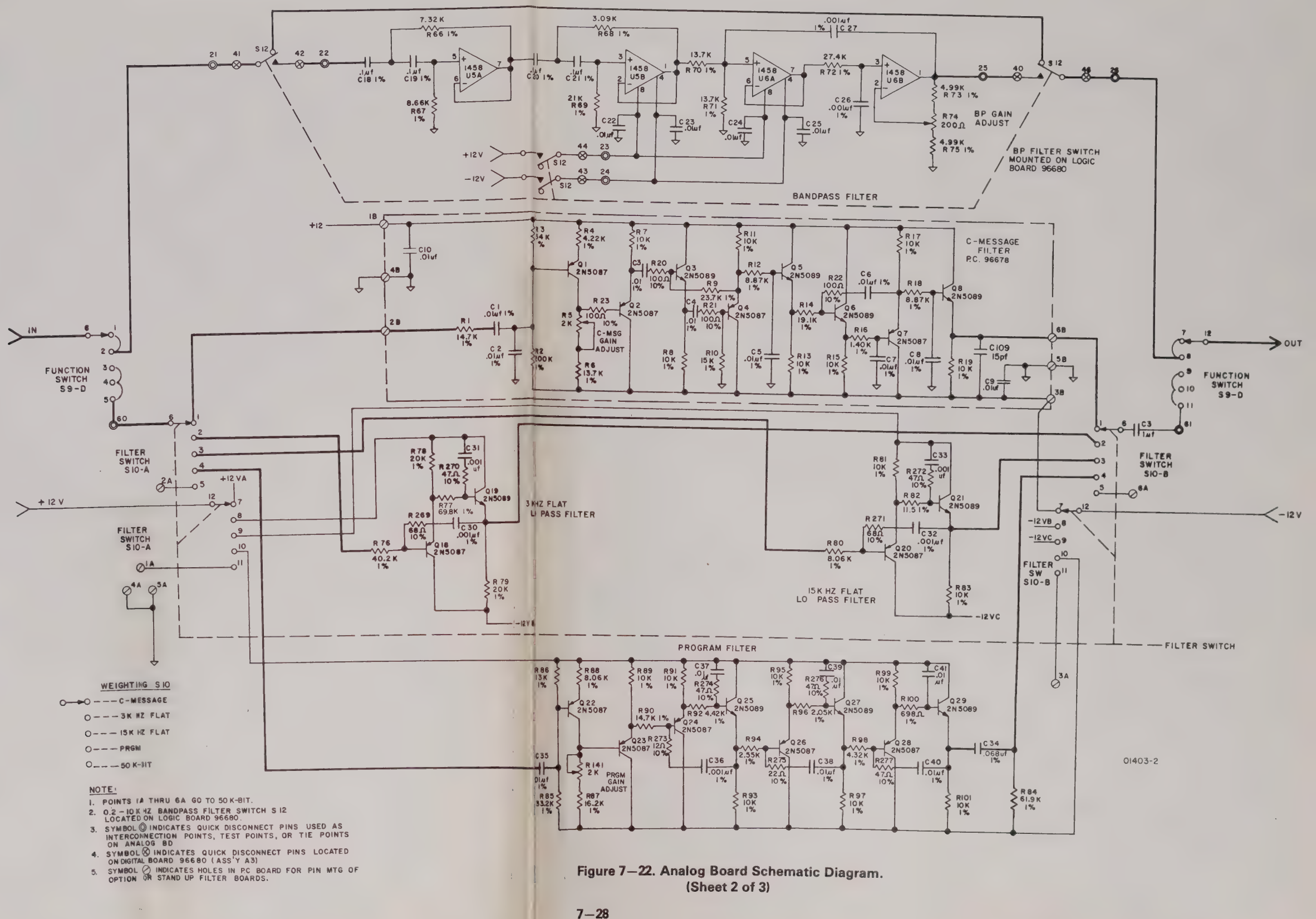
NOTES

1. R252 IS NOMINALLY 681Ω SELECTED FOR 900 IMP. AT 1KHZ
2. C91 IS NOMINALLY .082 UF, SELECTED FOR 900 IMP. AT 60KHz
3. SYMBOL ◎ INDICATES QUICK DISCONNECT PINS USED AS INTERCONNECTION POINTS, TEST POINTS, OR TIE POINTS.
4. ALL DIODES ARE IN4148 UNLESS OTHERWISE NOTED

ANALOG BOARD	
NE PART NO.	D4002-00-017
REF DESIG	A4
PC NO.	96666

01403-1

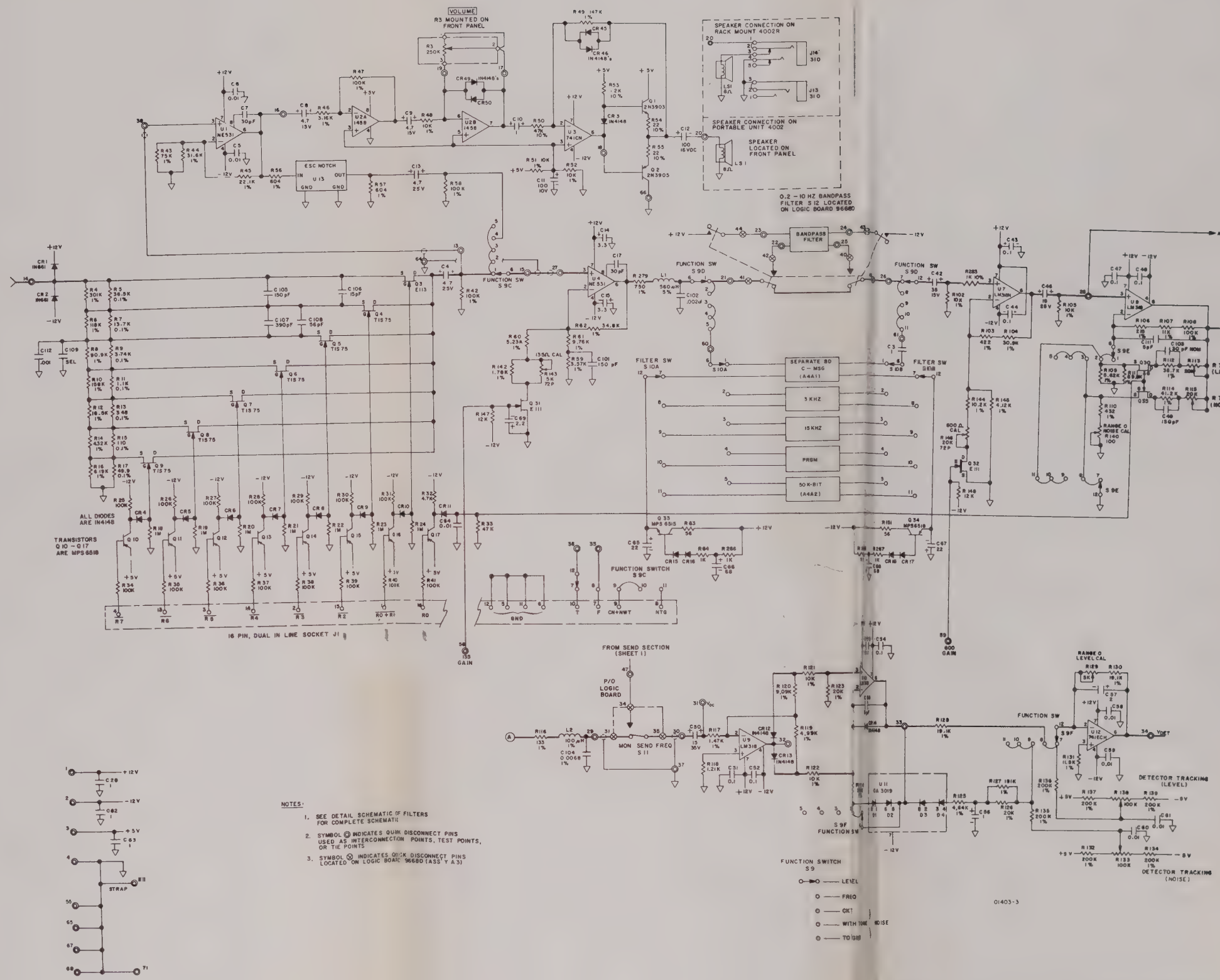
Figure 7—22. Analog Board Schematic Diagram. (Sheet 1 of 3)



NOTE:

1. POINTS 1A THRU 6A GO TO 50 K-BIT.
2. 0.2 – 10 K HZ BANDPASS FILTER SWITCH S 12 LOCATED ON LOGIC BOARD 96680.
3. SYMBOL ⓪ INDICATES QUICK DISCONNECT PINS USED AS INTERCONNECTION POINTS, TEST POINTS, OR TIE POINTS ON ANALOG BD
4. SYMBOL ⊗ INDICATES QUICK DISCONNECT PINS LOCATED ON DIGITAL BOARD 96680 (ASS'Y A3)
5. SYMBOL ⊘ INDICATES HOLES IN PC BOARD FOR PIN MTG OF OPTION OR STAND UP FILTER BOARDS.

Figure 7–22. Analog Board Schematic Diagram. (Sheet 2 of 3)

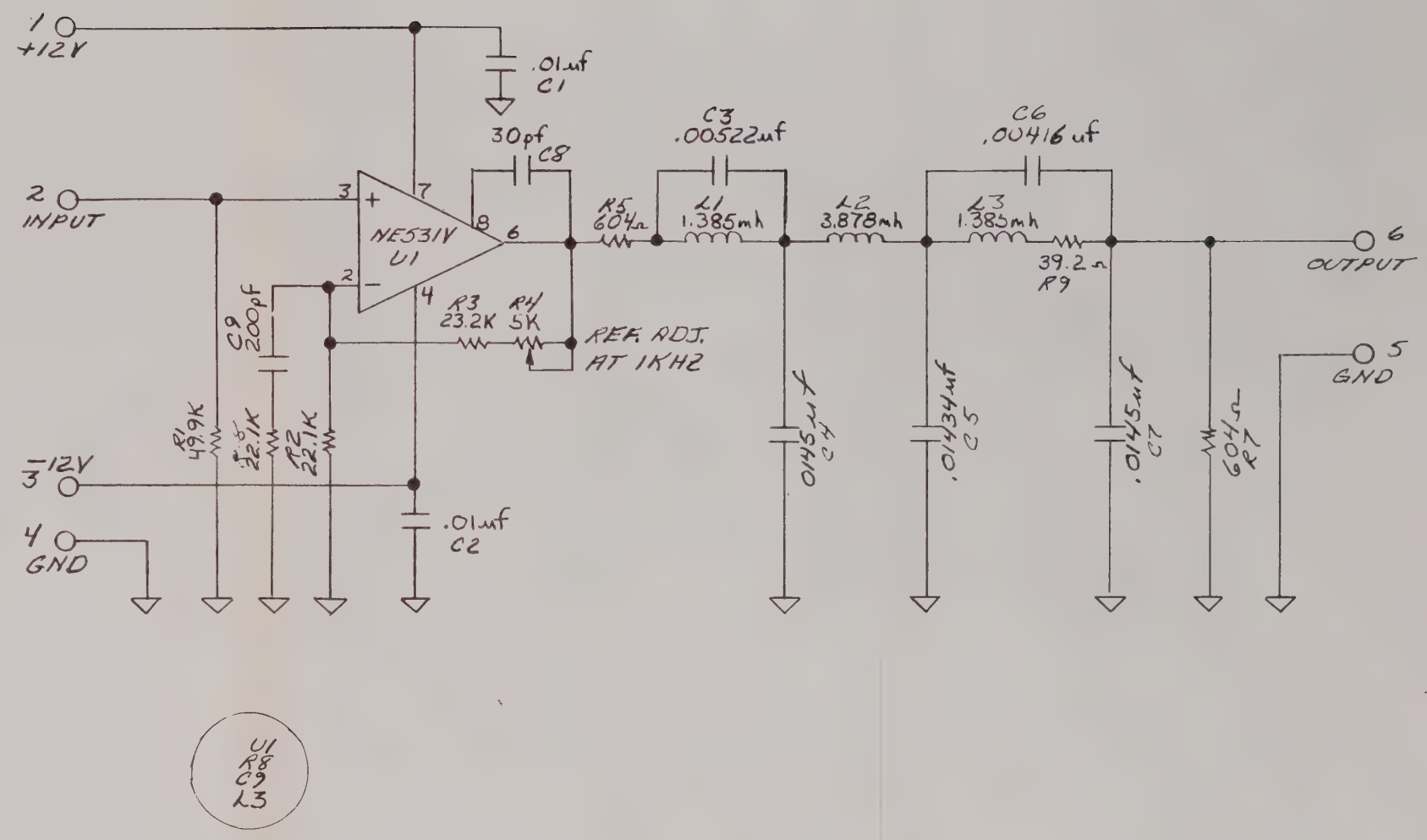


NOTES:

1. SEE DETAIL SCHEMATIC OF FILTERS FOR COMPLETE SCHEMATIC
2. SYMBOL ⊙ INDICATES QUIK DISCONNECT PINS USED AS INTERCONNECTION POINTS, TEST POINTS, OR TIE POINTS
3. SYMBOL ⊗ INDICATES QUICK DISCONNECT PINS LOCATED ON LOGIC BOARD 96680 (A53 Y A3)

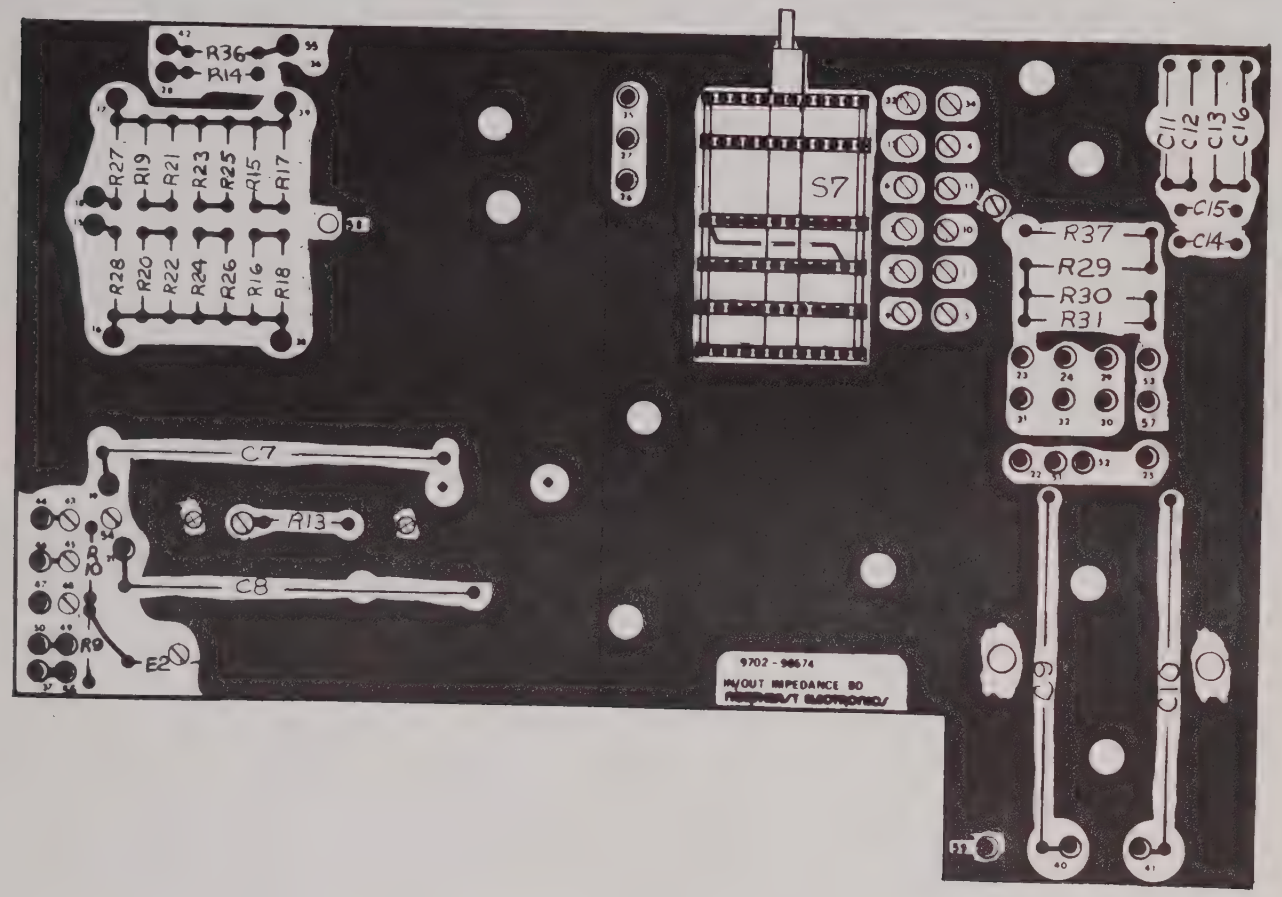
Figure 7–22. Analog Board Schematic Diagram. (Sheet 3 of 3)

Figure 7—23. 50-kb/s Filter Board Parts Location Diagram.



50-kb/s FILTER	
NE PART NO.	B4002-00-012
REF DESIG	A4A2
PC NO.	96809

Figure 7—24. 50-kb/s Filter Board Schematic Diagram.



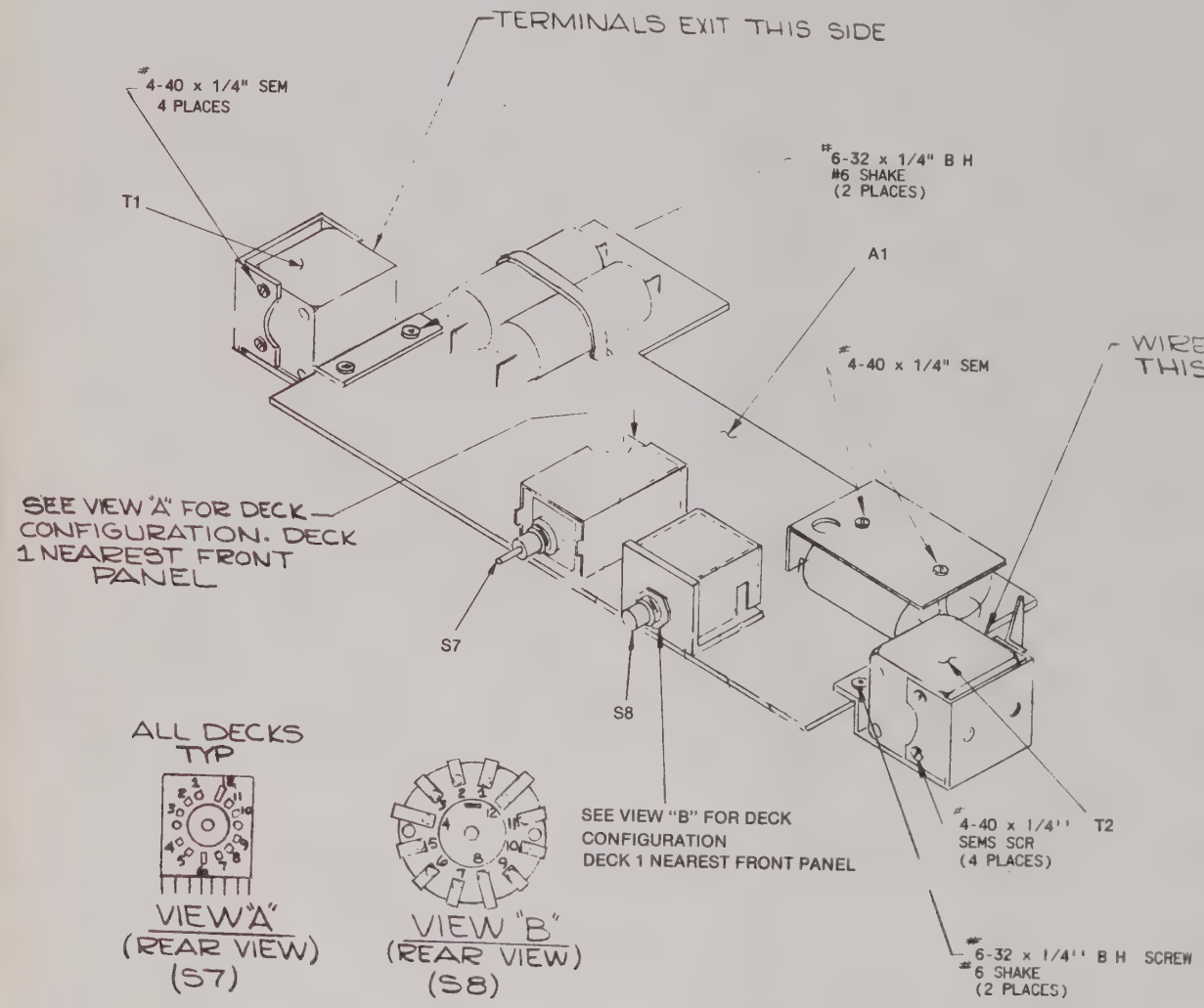
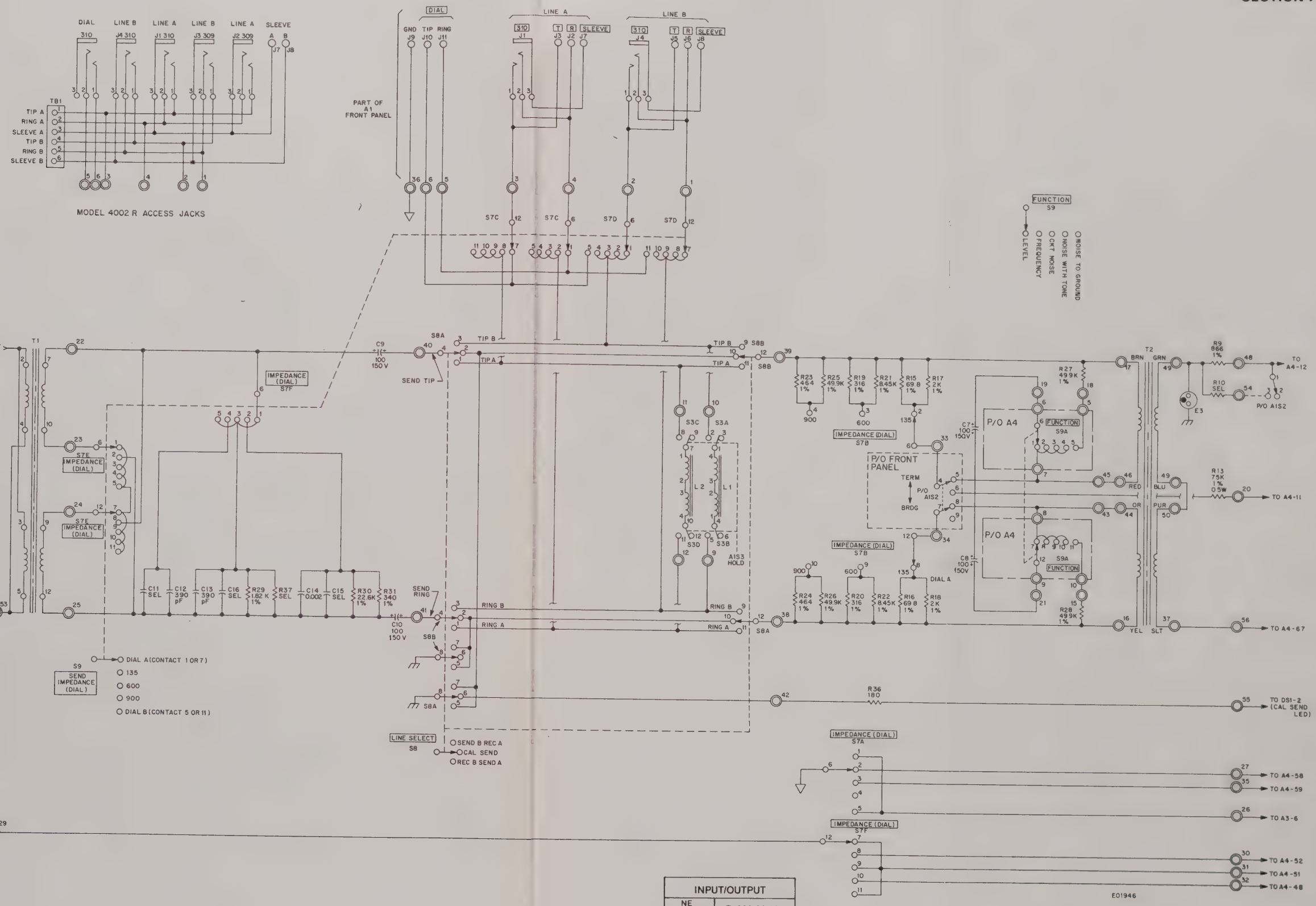


Figure 7—25. Input/Output Board Parts Location Diagram.



INPUT/OUTPUT	
NE PART NO.	E4002-00-324
REF DESIG	A5
PC NO.	96674

Figure 7—26. Input/Output Board Schematic Diagram.

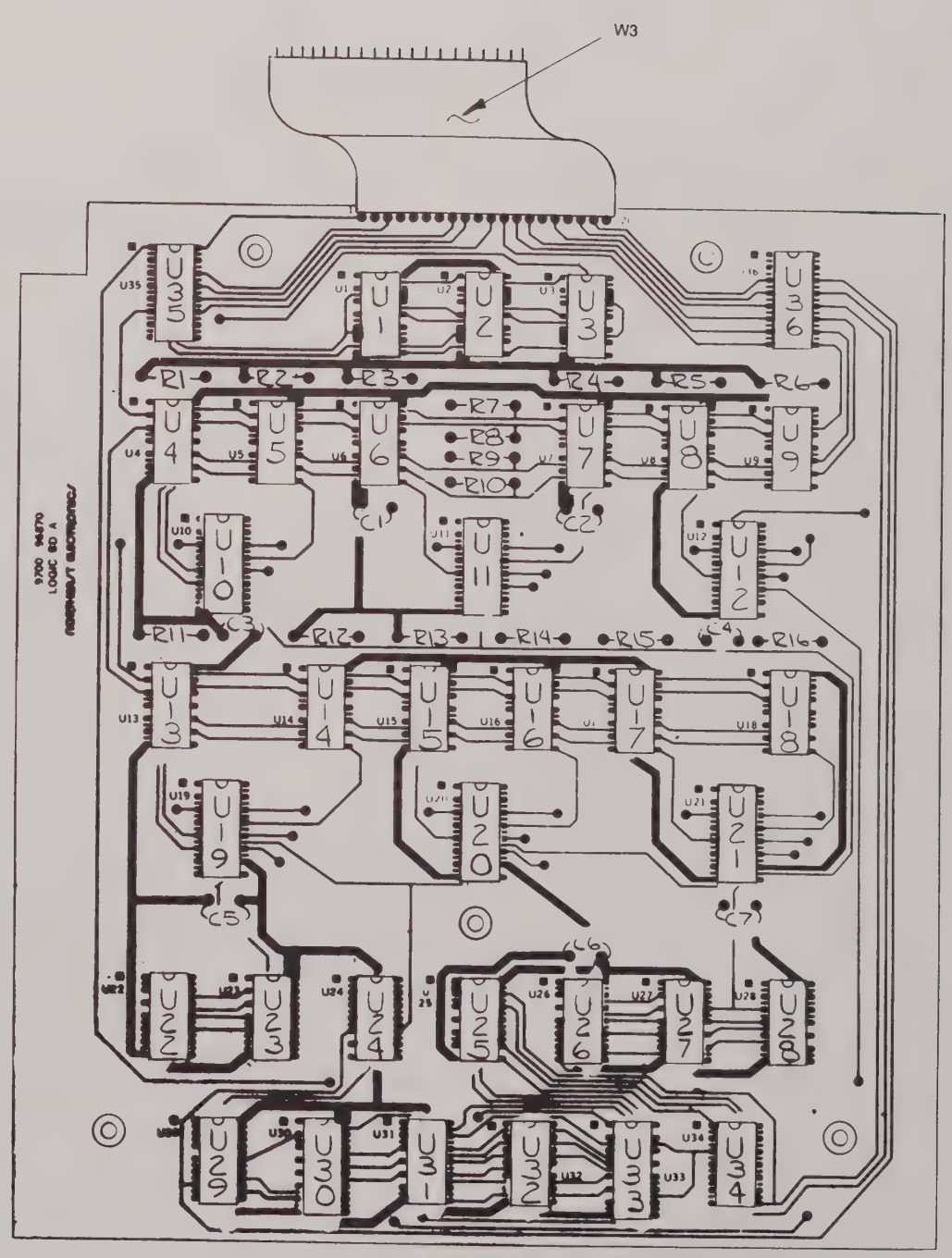
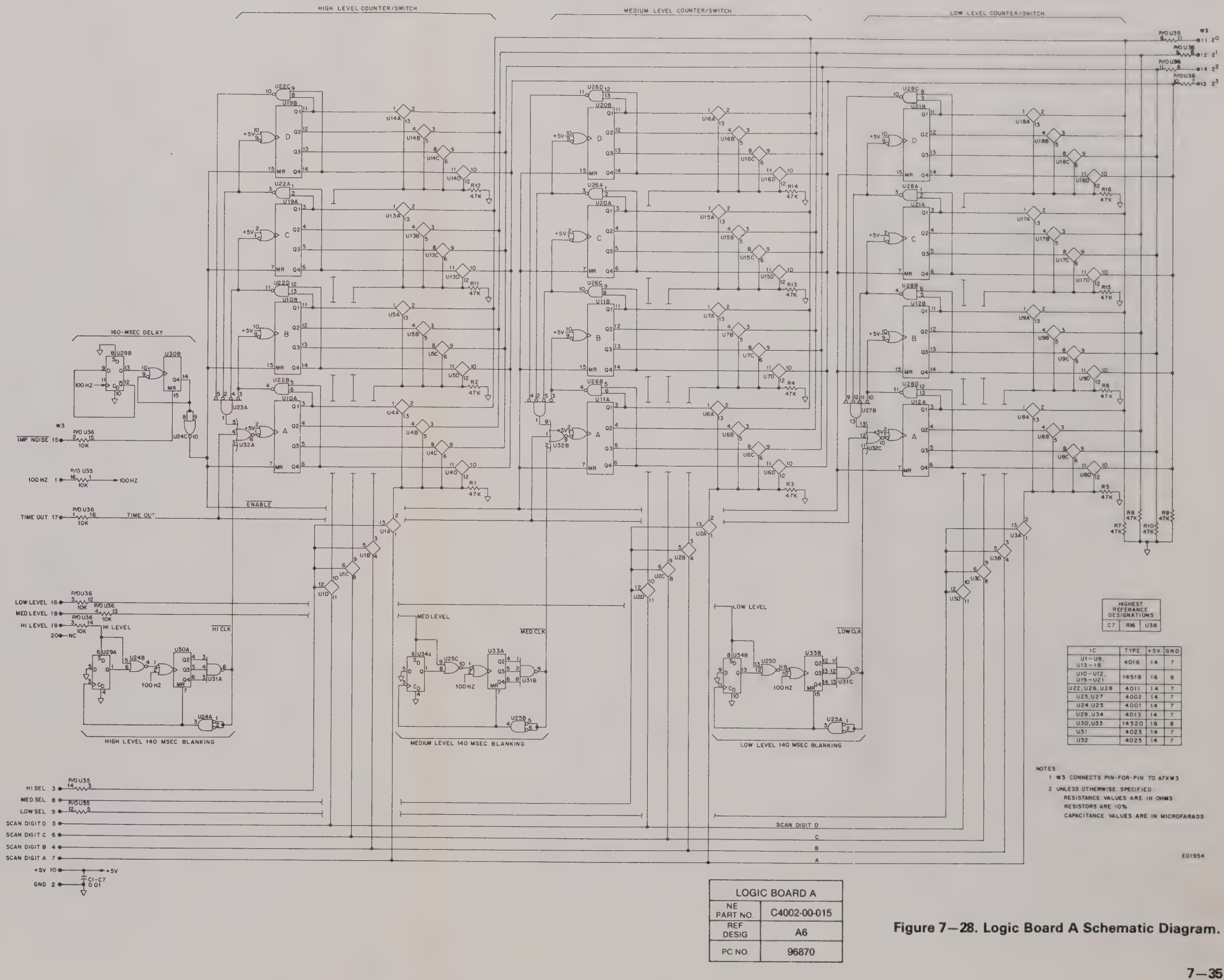


Figure 7—27. Logic Board A Parts Location Diagram.



HIGHEST REFERANCE DESIGNATIONS		
C7	R16	U36

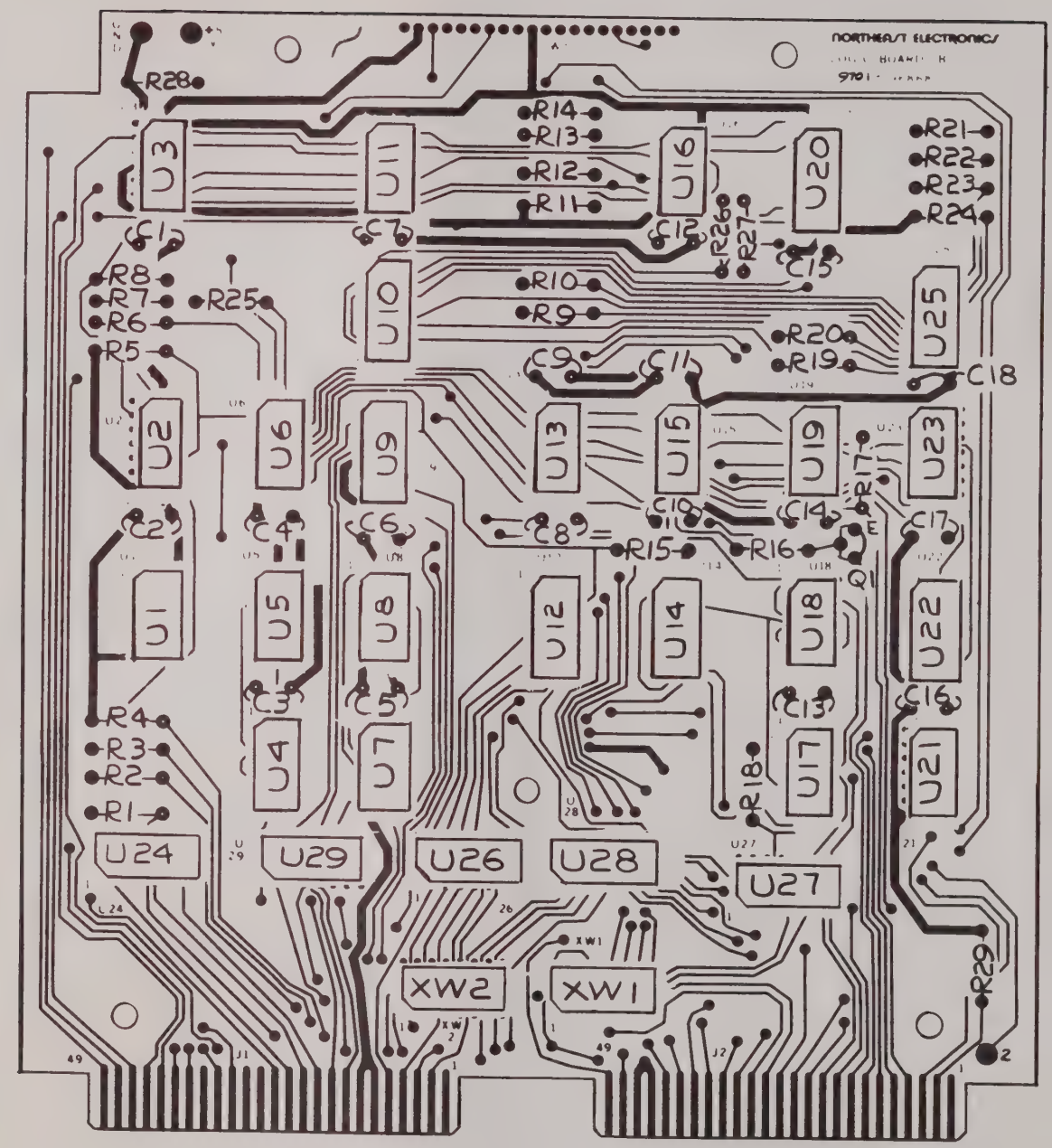
IC	TYPE	+5V	GND
U1–U9, U13–18	4016	14	7
U10–U12, U19–U21	14518	16	8
U22, U26, U28	4011	14	7
U23, U27	4002	14	7
U24, U25	4001	14	7
U29, U34	4013	14	7
U30, U33	14520	16	8
U31	4023	14	7
U32	4025	14	7

NOTES
1. W3 CONNECTS PIN-FOR-PIN TO A7XW3
2. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS
   RESISTORS ARE 10%
   CAPACITANCE VALUES ARE IN MICROFARADS

E01954

LOGIC BOARD A	
NE PART NO.	C4002-00-015
REF DESIG	A6
PC NO.	96870

Figure 7–28. Logic Board A Schematic Diagram.



• INDICATES LARGE QUICK DISCONNECT PINS. (3)

	STRAP PINS	TO
U4	12, 13	+5V
U6	5, 6	GND
U13	1, 2	GND
U23	12, 13	+5V

Figure 7—29. Logic Board B Parts Location Diagram.

DIVIDE-BY-6000 CIRCUIT

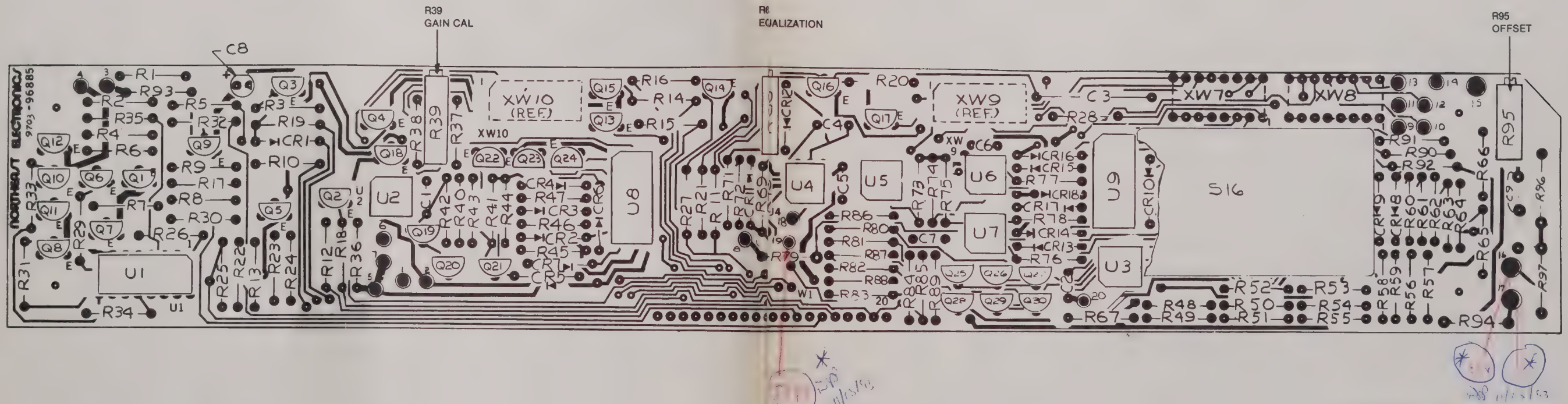
RECEIVER RANGE SELECT

IC	TYPE	+5V	GND
U1-3, U11, U16, U17	4016	14	7
U4, U8, U13	4011	14	7
U5, U15	4013	14	7
U6	4030	14	7
U7, U18, U19, U23	4001	14	7
U9, U12, U14	4019	16	8
U10, U20	4029	16	8
U21	4012	14	7
U22	4020	16	8
U24-U29 (10K)	898-3 R10K	–	–

HIGHEST REFERENCE DESIGNATIONS		
C18	Q1	R29
U29	XW2	J2

LOGIC BOARD B	
NE PART NO.	C4002-00-014
REF DESIG	A7
PC NO.	96868

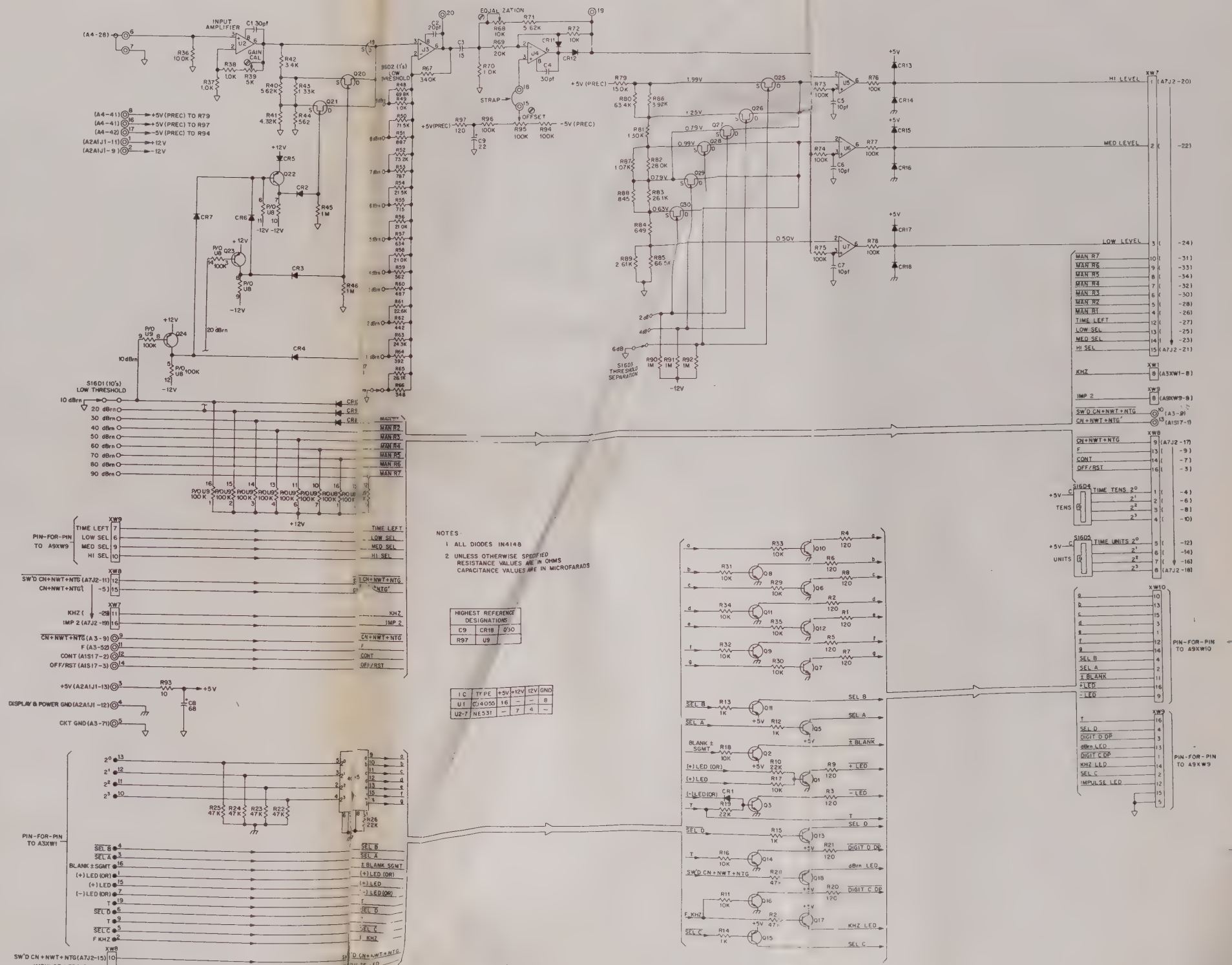
Figure 7—30. Logic Board B Schematic Diagram.



● DENOTES MALE QUICK DISCONNECT

CAUTION
CHANGES HAVE BEEN MADE
* ON THIS STAGE.
SEE ISSUE SHEET.

Figure 7—31. Display Driver Board Parts Location Diagram.



NOTES:
1. ALL DIODES IN4148
2. UNLESS OTHERWISE SPECIFIED RESISTANCE VALUES ARE IN OHMS CAPACITANCE VALUES ARE IN MICROFARADS

HIGHEST REFERENCE DESIGNATIONS		
C9	CR18	Q30
R97	U9	

I.C	TYPE	+5V	+12V	12V	GND
U1	CD4056	16	–	–	8
U2-7	NE531	–	7	4	–

DISPLAY DRIVER	
NE PART NO	D4002-00-016
REF DESIG	A3
PC NO	96885

Figure 7–32. Display Driver Board Schematic Diagram.

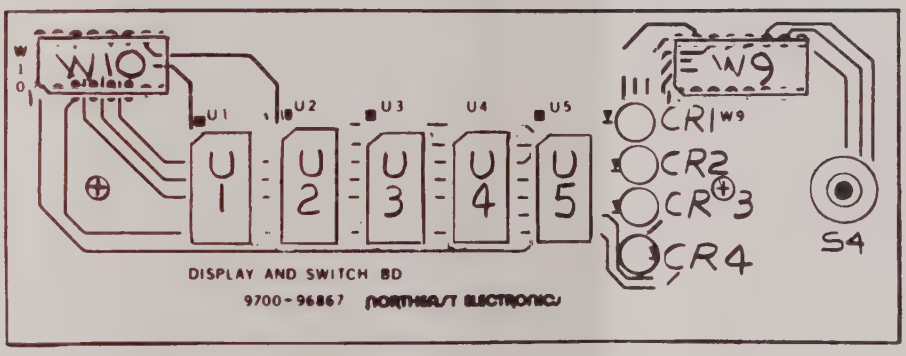
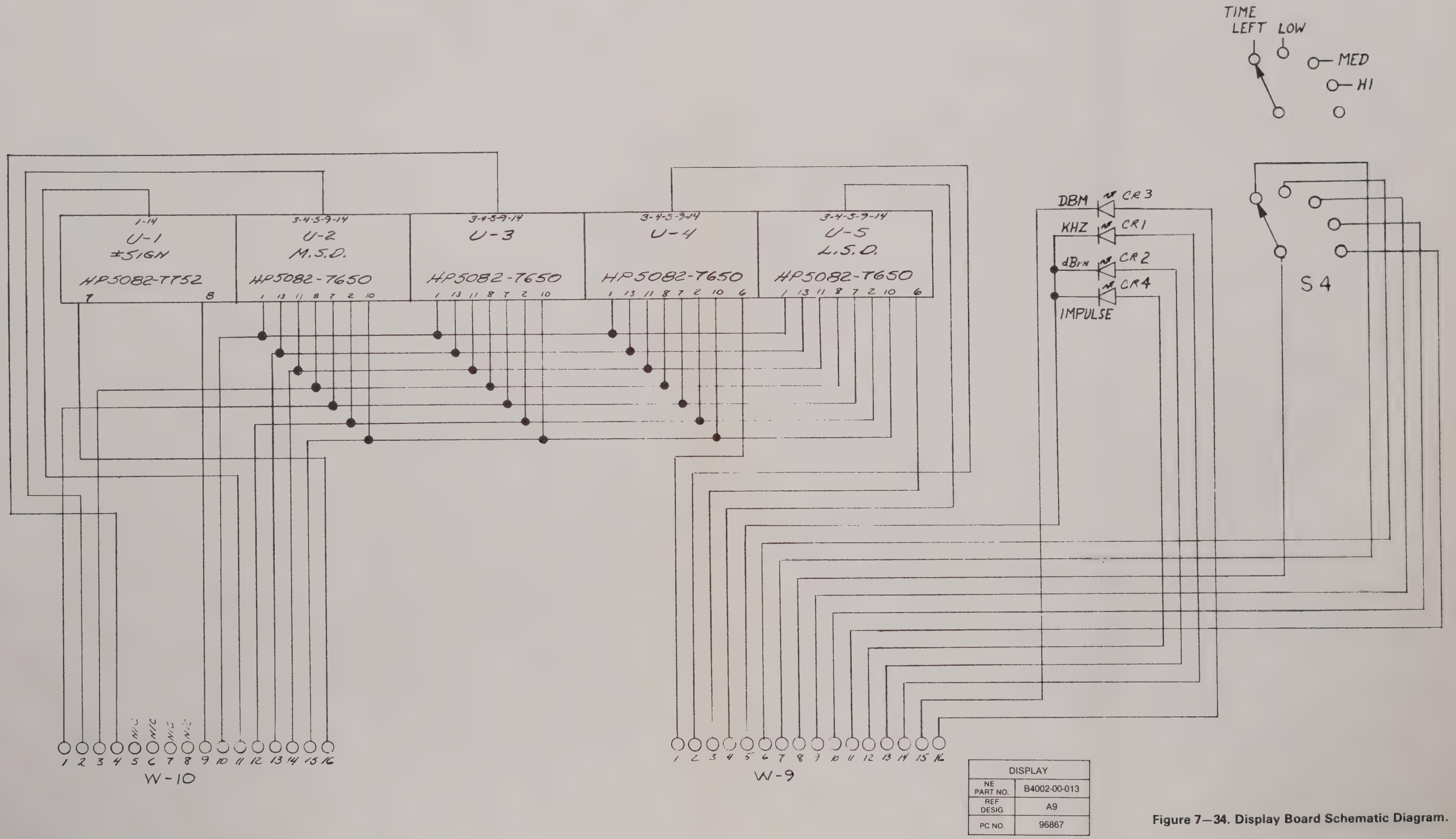


Figure 7—33. Display Board Parts Location Diagram.



DISPLAY	
NE PART NO.	B4002-00-013
REF DESIG	A9
PC NO.	96867

Figure 7—34. Display Board Schematic Diagram.

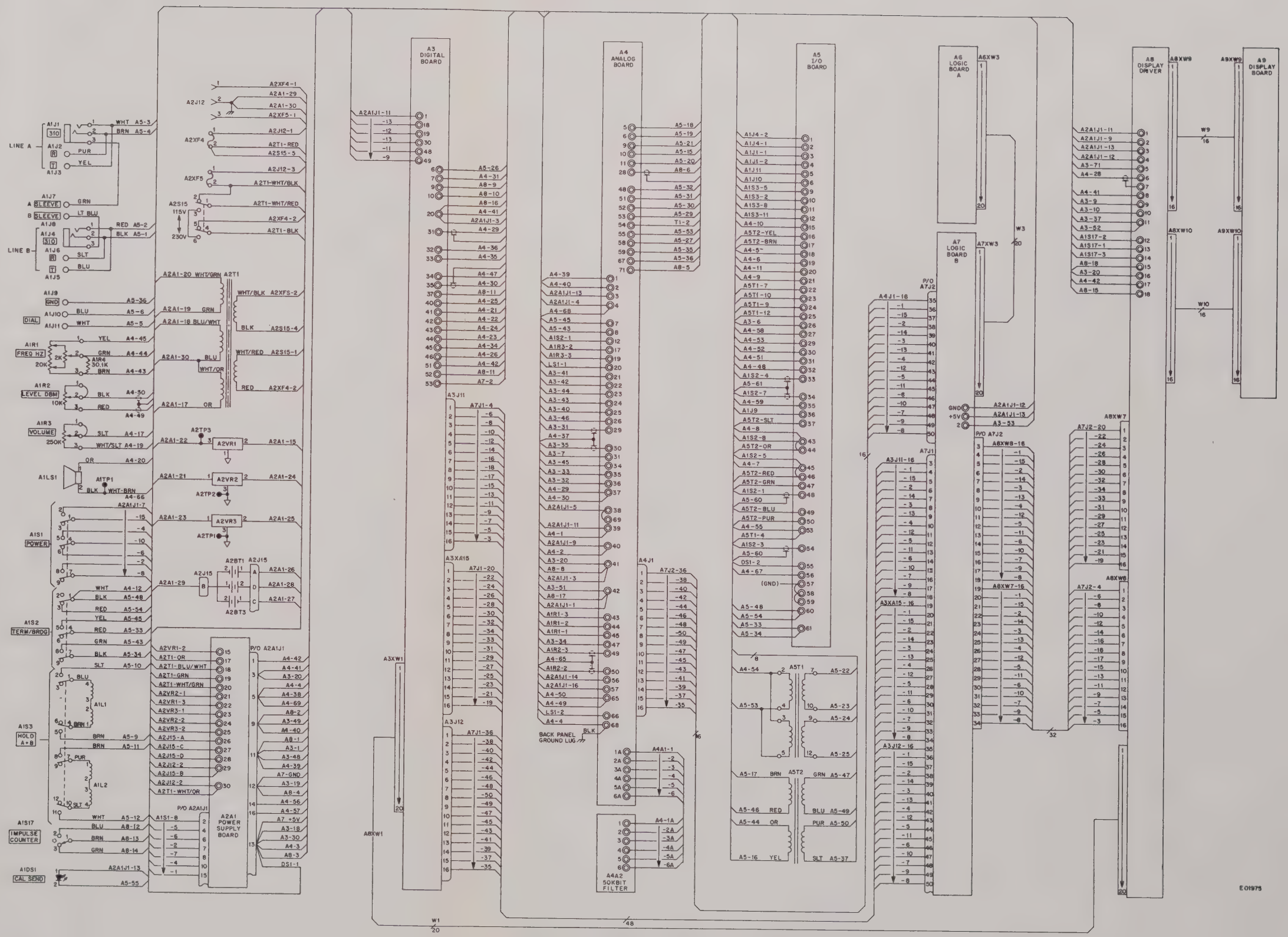


Figure 7—35. Model 4002 Wiring Diagram.

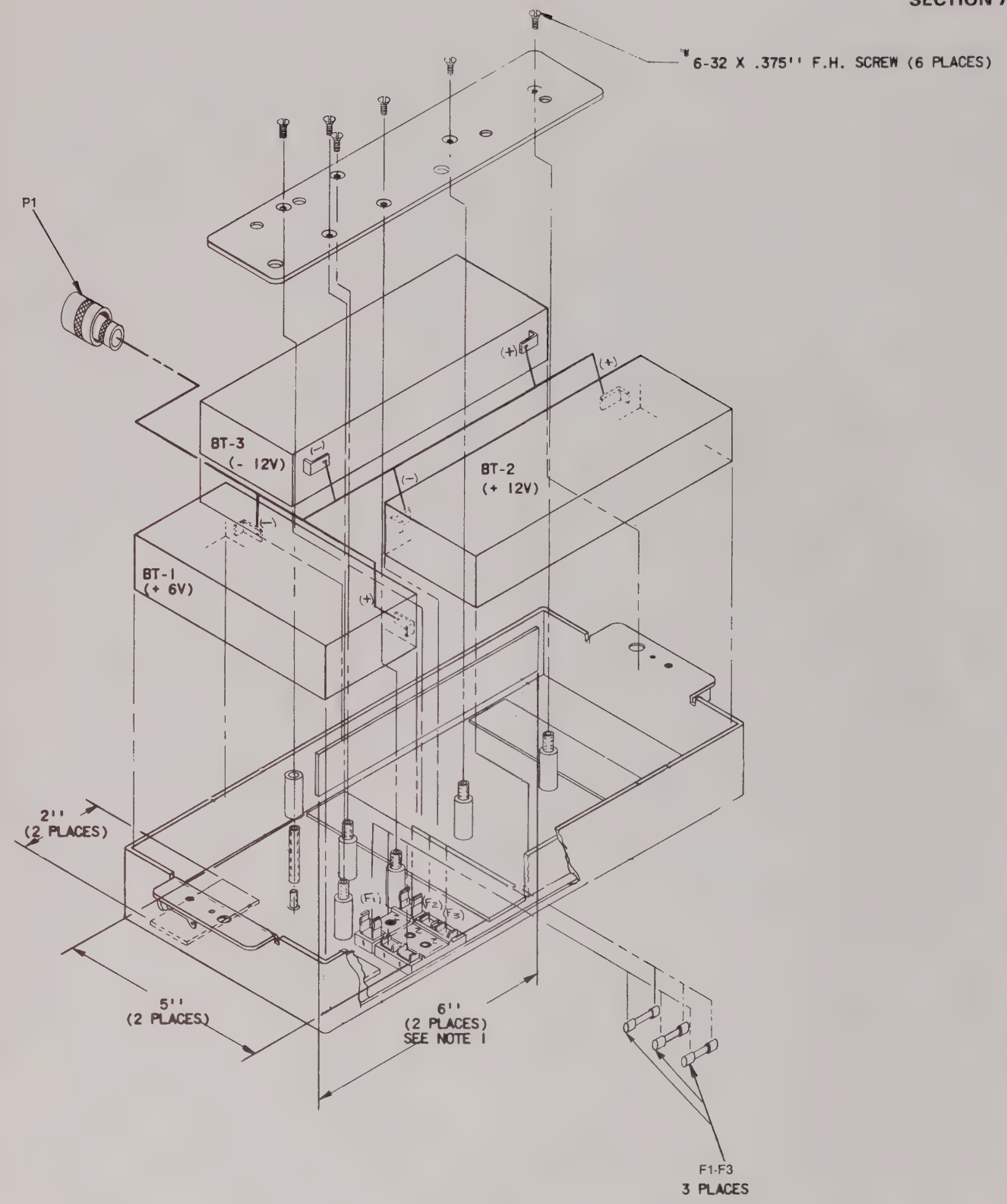


Figure 7—36. Optional Battery Pack Assembly Diagram.

SECTION 8

PARTS LISTS

8.1 This section contains parts lists for electronic components in the Model 4002 Transmission And Impulse Noise Distribution Set.

Table 8—1. Model 4002 Overall Assembly Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
A5	FINAL I/O BD ASSY A5						A400200024
DS1	W/LEADS	20MA		1.7V	INT-MARKET	L617R-100R	726100001
H5	HARNESS SHEET#5						A004400018
H6	HARNESS SHEET #6						A004400037
J1	WIRING ASSY J1,4						A004400043
J2	BINDING POST,BLACK				H.H. SMITH	1517-103	652400001
J3	BINDING POST,RED				H.H. SMITH	1517-102	652400002
J4	WIRING ASSY J1,4						A004400043
J5	BINDING POST,RED				H.H. SMITH	1517-102	652400002
J6	BINDING POST,BLACK				H.H. SMITH	1517-103	652400001
J7-8	BLACK NYLON PHONE				HH SMITH	241	650500100
J9	BINDING POST METAL GND				H H SMITH	137SP	652500100
J10-11	CLIP POST						A012500107
L1-2	4H				NEWTON	TN-1274	450200200
LS1	8-	.1W			PHILMORE	TS19	926000015
MP2	3/4 HIGH				AIR	1743W	836500001
PC4	PC ASSY 96867 DISPLAY BD						A400200013
PC10	PC ASSY 96885 DISPLAY DRV						A400200015
R1	20K	LINEAR	3%		DE YOUNG	MODEL 23A	240102030
R2	10 K	2 W	5%		SPECTROL	534	233101031
R3	250K		20%		AB	70A4N048R254A	232002541
R4	30.1K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220230121
S1	3PDT				C&K	7301P3Y1ZB	620401201
S2	WIRING ASSY S2						A004400040
S3	WIRING ASSY S3						A004400041
S17	SPDT	5A		28V	C+K COMP	7103P3DZB	620400300
W1	HARNESS SHEET #2						A004400012

Table 8—2. 50-kb/s Filter (A4A2) Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1-2	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
C3	.00522UF		2%	100V	WESCO	32M5221G-1	322152210
C4-5	.0144UFD		1%	100V	WESCO	32M1442F-1	322114420
C6	.00416UF		1%	50V	WESCO	32M4161F-05	322141610
C7	.0144UFD		1%	100V	WESCO	32M1442F-1	322114420
C8	30PF		2%	500V	ELMENCO	CM04ED300GO-	335403000
C9	200PF		5%	500V	C.DUBILIER	CM05FD201J03	335402010
L1	1.385MH		1%		ARTTED	9231	460100002
L2	3.878MH		1%		ARTTED	9232	460100003
L3	1.385MH		1%		ARTTED	9231	460100002
R1	49.9K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249921
R2	22.1K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220222121
R3	23.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220223221
R4	5K	1/2W	10%	200V	HELIPOT	72XWR5K	232705020
R5	604-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220260401
R7	604-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220260401
R8	22.1K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220222121
R9	39.2-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220239291
U1	8PDIL			22V	SIGNETICS	NE531	500005310

Table 8—3. Display Board (A9) Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
CR1-4		12MA		5V	H.PACKARD	5082-4860	564500900
S4	SWITCH,PC MTG MINI				GRAYHILL	50CP36-01-1-4N	640001200
U1	14PDIL	20MA RED			HP	5082-7752	728301702
U2-5	14PDIL	20MA RED			HP	5082-7650	728301701
W9-10	FLAT CABLE CONN. 16 PIN						A400200019
XU1-5	14DILP				AUGAT	314-AG5D-2R	820100500

Table 8—4. Logic Board B (A7) Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1-18	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
Q1	TO-92	350MW TA PNP		40V	MOTOROLA	MPS6518	550065180
R1-21	47K	1/4W	10%		AB	TYPE CB	200104736
R22	10K	1/4W	10%		2	00 A410100015R71-7	200101036
R23-24	47K	1/4W	10%		AB	TYPE CB	200104736
R25-29	10K	1/4W	10%		2	00 A410100015R71-7	200101036
U1-3	14DIP-P	B			CMOS RCA	CD4016	510004016
U4	14DIP-P	B			CMOS RCA	CD4011	510004011
U5	14DIP-P	B			CMOS RCA	CD4013	510004013
U6	14DIP-P	B			CMOS RCA	CD4030	510004030
U7	14DIP-P	B			CMOS RCA	CD4001	510004001
U8	14DIP-P	B			CMOS RCA	CD4011	510004011
U9	16DIP-P	B			CMOS RCA	CD4019	510004019
U10	16DIP-P	B			CMOS RCA	CD4029	510004029
U11	14DIP-P	B			CMOS RCA	CD4016	510004016
U12	16DIP-P	B			CMOS RCA	CD4019	510004019
U13	14DIP-P	B			CMOS RCA	CD4011	510004011
U14	16DIP-P	B			CMOS RCA	CD4019	510004019
U15	14DIP-P	B			CMOS RCA	CD4013	510004013
U16-17	14DIP-P	B			CMOS RCA	CD4016	510004016
U18-19	14DIP-P	B			CMOS RCA	CD4001	510004001
U20	16DIP-P	B			CMOS RCA	CD4029	510004029
U21	14DIP-P	B/UB			CMOS RCA	CD4012	510004012
U22	16DIP-P	B			CMOS RCA	CD4020	510004020
U23	14DIP-P	B			CMOS RCA	CD4001	510004001
U24-29	16 DILP	TYPE 3	2%	100	BECKMAN	898-3-R10K	514500102
XW1	SKT IC 15P PC				AUGAT	316-AG5D-2R	820100400
XW2	SKT IC 16P PC				AUGAT	316-AG5D-2R	820100400
*	CABLE TO J1-50PIN				TAPE ASSY		
*	" J2 "				"		

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Table 8—5. Logic Board A (A6) Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1-7	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
R1-16	47K	1/4W	10%		AB	TYPE CB	200104736
U1-9	14DIP-P	B			CMOS RCA	CD4016	510004016
U10-12	16 DIP-P	B			CMOS MOTOROLA	MC14518	510004518
U13-18	14DIP-P	B			CMOS RCA	CD4016	510004016
U19-21	16 DIP-P	B			CMOS MOTOROLA	MC14518	510004518
U22	14DIP-P	B			CMOS RCA	CD4011	510004011
U23	14DIP-P	B			CMOS RCA	CD4002	510004002
U24-25	14DIP-P	B			CMOS RCA	CD4001	510004001
U26	14DIP-P	B			CMOS RCA	CD4011	510004011
U27	14DIP-P	B			CMOS RCA	CD4002	510004002
U28	14DIP-P	B			CMOS RCA	CD4011	510004011
U29	14DIP-P	B			CMOS RCA	CD4013	510004013
U30	16 DIP-P	B			CMOS MOTOROLA	MC14520	510004520
U31	14DIP-P	B/UB			CMOS RCA	CD4023	510004023
U32	14DIP-P	B/UB			CMOS RCA	CD4025	510004025
U33	16 DIP-P	B			CMOS MOTOROLA	MC14520	510004520
U34	14DIP-P	B			CMOS RCA	CD4013	510004013
U35-36	16 DILP	TYPE 3	2%	100	BECKMAN	898-3-R10K	514500102
* W1	20 PIN RIBBON						

THREE NOTES CAUTION CHANGES HAVE BEEN MADE ON THIS PAGE. SEE ISSUE SHEET. 11/15/93

(DEAD PIG)

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Table 8—6. Display Driver Board (A8) Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1	30PF		2%	500V	ELMENCO	CM04ED300GO-	335403000
C2	20PF		5%	100V	ELMENCO	CM04EA200JO	335402000
C3	15UF		20%	35V	TSI	PA15HH35NPT	301301560
C4	30PF		2%	500V	ELMENCO	CM04ED300GO-	335403000
C5-7	10PF		5%	100V	ELMENCO	CM04-A100JO-	335401000
C8	68UF		10%	15V	KEMET	T362C686K015AS	310506860
C9	22UF		10%	6V	KEMET	T330A226K006AS	310002260
CR1-18	D035	4NS 10MA	SI	50UA	FAIRCHILD	IN4148	560041480
Q1	TO-92	350MW TA	NPN	25V	MOTOROLA	MPS6515	550065150
Q2	TO-92	350MW TA	PNP	40V	MOTOROLA	MPS6518	550065180
Q3	TO-92	350MW TA	NPN	25V	MOTOROLA	MPS6515	550065150
Q4-5	TO-92	350MW TA	PNP	40V	MOTOROLA	MPS6518	550065180
Q6-12	TO-92	350MW TA	NPN	25V	MOTOROLA	MPS6515	550065150
Q13	TO-92	350MW TA	PNP	40V	MOTOROLA	MPS6518	550065180
Q14	TO-92	350MW TA	NPN	25V	MOTOROLA	MPS6515	550065150
Q15	TO-92	350MW TA	PNP	40V	MOTOROLA	MPS6518	550065180
Q16-18	TO-92	350MW TA	NPN	25V	MOTOROLA	MPS6515	550065150
Q19-21	MODTO92	360MW TA	N	30V	TI	T1S75	554000750
Q22-24	TO-92	350MW TA	PNP	40V	MOTOROLA	MPS6518	550065180
Q28-30	MODTO92	360MW TA	N	30V	TI	T1S75	554000750
R1-9	120-	1/4W	10%		AB	TYPE CB	200101216
R10	22K	1/4W	10%		AB	TYPE CB	200102236
R11	10K	1/4W	10%		2	00 A410100015R71-7	200101036
R12-15	1K	1/4W	10%		AB	TYPE CB	200101026
R16-18	10K	1/4W	10%		2	00 A410100015R71-7	200101036
R19	22K	1/4W	10%		AB	TYPE CB	200102236
R20-21	120-	1/4W	10%		AB	TYPE CB	200101216
R22-25	47K	1/4W	10%		AB	TYPE CB	200104736
R26	22K	1/4W	10%		AB	TYPE CB	200102236
R27-28	47K	1/4W	10%		AB	TYPE CB	200104736
R29-35	10K	1/4W	10%		2	00 A410100015R71-7	200101036
R36	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R37-38	1000-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210011
R39	5K	.75W	10		HELIPOT	89PR5K	232505020
R40	5.62K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220256211
R41	4320-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220243211
R42	3400-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220234011
R43	1330-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220213311
R44	562-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220256201
R45-47	1M	1/4W	10%		AB	TYPE CB	200101056
R48	69.8K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220269821
R49	1000-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210011
R50	71.5K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220271521
R51	8887-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220288701
R52	73.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220273221
R53	787-	108W	1%		ELECTRA	RN55 SIZE 100 PPM	220278701
R54	21.5K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220221521
R55	715-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220271501
R56	21K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220221021
R57	634-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220263401

Table 8—6. (Cont'd).

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
R58	21K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220221021
R59	562-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220256201
R60	487-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220248701
R61	22.6K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220222621
R62	442-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220244201
R63	24.3K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220224321
R64	392-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220239201
R65	26.1K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220226121
R66	348-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220234801
R67	34K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220234021
R68	10K	.75W	10%		HELIPOT	89PR10K	232501030
R69	20K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220021
R70	1000-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210011
R71	5.62K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220256211
R72	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R73-78	100K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210031
R79	15K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220215021
R80	63.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220263421
R81	1300-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220213011
R82	28K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220228021
R83	26.1K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220226121
R84	649-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220264901
R85	66.5K	1/8W	1%	1	ELECTRA	RN55 SIZE 100 PPM	220266521
R86	3.92K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220239211
R87	1070-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210711
R88	845-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220284501
R89	2610-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220226111
R90-92	1M	1/4W	10%		AB	TYPE CB	200101056
R93	10-	1/2W	10%		AB	TYPE EB	200201006
R94	100K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210031
R95	100K	.75W	10%		HELIPOT	89PR100K	232501040
R96	100K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210031
R97	120-	1/4W	10%		AB	TYPE CB	200101216
S16	THUMBWHEEL SW,5SECT.PC MT				DIGITRAN	29-N-18	626801100
U1	16DIP-2	B		CMOS	RCA	CD4055	510004055
U2-7	8PDIL			22V	SIGNETICS	NE531	500005310
U8-9	16 DILP	TYPE 3	2%	100	BECKMAN	898-3-R100K	514500107
XW7-10	16 DIP				BURNDY	DILB16P-108	820101100

Table 8—7. Analog Board (A4) Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
A1	96678 C-MSG FILTER A4A1						A004400026
C1-2	1 UF			200V	SPRAGUE	500D105F200337	300901050
C3	1UF	Z5U TC	20%	50V	SPRAGUE	5C023105X0500C5	330501050
C4	4.7UF		20%	25V	TSI	PA4.7EE25NPT	301304750
C5-6	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
C7	30PF		2%	500V	ELMENCO	CM04ED300GO-	335403000
C8-9	4.7UF		20%	25V	TSI	PA4.7EE25NPT	301304750
C10	1UF	Z5U TC	20%	50V	SPRAGUE	5C023105X0500C5	330501050
C11	100UF	F	10%	10V	SPRAGUE	196D107X9010PE4	310801070
C12	100UF			16V	SPRAGUE	TE-1162	300201071
C13	4.7UF		20%	25V	TSI	PA4.7EE25NPT	301304750
C14-15	3.3UF		10%	25V	KEMET	T330A335K025AS	310003350
C16	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
C17	30PF		2%	500V	ELMENCO	CM04ED300GO-	335403000
C18-21	.1UF		1%	100V	F-DYNE	PPA-11-.1-100-1	322401040
C22-25	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
C26-27	.001UF		1%	100V	F-DYNE	PPA-11-.001-100-1	322401020
C28	1UF		10%	35V	KEMET	T330A105K035AS	310001051
C30-33	.001UF		1%	100V	F-DYNE	PPA-11-.001-100-1	322401020
C34	.068UF		1%	100V	F-DYNE	PPA-11-.068-100-1	322306830
C35	.01UF		1%	100V	FDYNE	PPA-11-.01-100-1	322401030
C36	.001UF		1%	100V	F-DYNE	PPA-11-.001-100-1	322401020
C37-41	.01UF		1%	100V	FDYNE	PPA-11-.01-100-1	322401030
C42	35UF		20%	15V	TSI	PA35HH15NPT	301303560
C43-44	.1UF		10%	50V	KEMET	T330A104K050AS	310001040
C46	15UF		20%	35V	TSI	PA15HH35NPT	301301560
C47-48	.1UF		00	75V	CENTRALAB	DDA-104	330201040
C49	150PF		2%	500V	ELMENCO	CM05-D151GO	335401510
C50	15UF		20%	35V	TSI	PA15HH35NPT	301301560
C51-54	.1UF		00	75V	CENTRALAB	DDA-104	330201040
C55	5PF		10%	500	ELMENCO	CM04-D050DO-	335400500
C56	1UF	Z5U TC	20%	50V	SPRAGUE	5C023105X0500C5	330501050
C57	2UF			25V	SPRAGUE	TE1201	300202051
C58-61	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
C62-63	1UF		10%	35V	KEMET	T330A105K035AS	310001051
C64	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
C65	22UF	F	20%	35V	SPRAGUE	196D226X0035PE4	310802261
C66	68UF	F	10%	15V	SPRAGUE	196D 686X901 5PE4	310806861
C67	22UF	F	20%	35V	SPRAGUE	196D226X0035PE4	310802261
C68	68UF	F	10%	15V	SPRAGUE	196D 686X901 5PE4	310806861
C69	2.2UF		10%	35V	KEMET	T330A225K035AS	310002250
C70	.05 UF		1%	100V	F-DYNE	PPA-11-.05-100-1	322405031
C71	SELVAL		10%		SPRAGUE	225P	320000000
C72	.0047 UF		1%	100V	F-DYNE	PPA-11-.0047-100-1	322404721
C73	SELVAL		10%		SPRAGUE	225P	320000000
C74	SEL.VAL.				ELMENCO	SEL.VAL.	335400000
C75	330PF		5%	100V	ELMENCO	CM04-A331JO-	335403310
C76-78	.1UF		20%	100V	VITRAMON	VK33BW104M	331001040
C79	.0015UF		10%	100V	SPRAGUE	225P15291WD3	320001520
C80	20PF		5%	100V	ELMENCO	CM04EA200JO	335402000
C81-82	270PF		2%	300V	ELMENCO	CM04EC271GO	335402711
C83-84	SEL.VAL.				ELMENCO	SEL.VAL.	335400000

Table 8—7. (Cont'd).

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C85	22PF		5%	500V	ELMENCO	CM15-C220J	335002200
C86	56PF		2%	500V	ELMENCO	CM04ED560G03	335405600
C87-88	100UF			16V	SPRAGUE	TE-1162	300201071
C89	20PF		5%	100V	ELMENCO	CM04EA200J0	335402000
C89	56PF		2%	500V	ELMENCO	CM04ED560G03	335405600
C90	200UF			16V	SPRAGUE	TE1164	300202070
C91	SEL.VAL.				ELMENCO	SEL.VAL.	335400000
C92	.082UF		10%	100V	SPRAGUE	225P82391WD3	320008230
C93-94	50UF			16V	SPRAGUE	TE1160	300205060
C95-98	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
C99-100	22UF	E	20%	25V	KEMET	T362C226M025AS	310402260
C101	150PF		2%	500V	ELMENCO	CM05-D151G0	335401510
C102	.002UF		10%	100V	SPRAGUE	225P20291WD3	320002020
C103	30PF		2%	500V	ELMENCO	CM04ED300G0-	335403000
C104	.0068 UF		1%	100V	F-DYNE	PPA-11-.0068-100-1	322406821
C105	150PF		2%	500V	ELMENCO	CM05-D151G0	335401510
C106	15PF		.5P	500V	ELMENCO	CM04-D150D03	335401500
C107	390 PF		2%	500V	ELMENCO	CM04DD391G0	335403910
C108	56PF		2%	500V	ELMENCO	CM04ED560G03	335405600
C109	SEL.VAL.				ELMENCO	SEL.VAL.	335400000
C111	5PF		10%	500	ELMENCO	CM04-D050D0-	335400500
C112	.001UF		1%	100V	F-DYNE	PPA-11-.001-100-1	322401020
C114-115	SELVAL		10%		SPRAGUE	225P	320000000
CR1-2	A1 300N 30M		SI	.1MA	TI	1N661	560006610
CR3-18	D035 4NS 10MA		SI	50UA	FAIRCHILD	IN4148	560041480
CR20-37	D035 4NS 10MA		SI	50UA	TI	1N4152	560041520
CR38-42	D035 4NS 10MA		SI	50UA	FAIRCHILD	IN4148	560041480
CR45-50	D035 4NS 10MA		SI	50UA	FAIRCHILD	IN4148	560041480
E1	PROTECTOR S/V GAS				SIEMENS	B1-C90/20	566009020
FL-1	1010 HZ				ESC ELECT.	ESC 42F86	470100700
J1	SKT IC 16P PC				AUGAT	316-AG5D-2R	820100400
L1	560 UH		5%		NYTRONICS	WEE 560	461000001
L2	100UH		5%		NYTRONICS	WEE-100	461000600
Q1	TO-92 350MW TA	NPN	40V		MOTOROLA	2N3903	550039030
Q2	TO92 350MW TC	PNP	40V		MOTOROLA	2N3905	552039050
Q3	TO106 350MW TA	N	35V		SILICONIX	E113	554000301
Q4-9	MODTO92 360MW TA	N	30V		TI	T1S75	554000750
Q10-17	TO-92 350MW TA	PNP	40V		MOTOROLA	MPS6518	550065180
Q18	TO92 350MW TC	PNP	50V		MOTOROLA	2N5087	552050870
Q19	TO-92 350MW TA	NPN	25V		MOTOROLA	2N5089	550050890
Q20	TO92 350MW TC	PNP	50V		MOTOROLA	2N5087	552050870
Q21	TO-92 350MW TA	NPN	25V		MOTOROLA	2N5089	550050890
Q22-24	TO92 350MW TC	PNP	50V		MOTOROLA	2N5087	552050870
Q25	TO-92 350MW TA	NPN	25V		MOTOROLA	2N5089	550050890
Q26	TO92 350MW TC	PNP	50V		MOTOROLA	2N5087	552050870
Q27	TO-92 350MW TA	NPN	25V		MOTOROLA	2N5089	550050890
Q28	TO92 350MW TC	PNP	50V		MOTOROLA	2N5087	552050870

Table 8—7. (Cont'd).

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
Q29	TO-92	350MW	TA NPN	25V	MOTOROLA	2N5089	550050890
Q30	MODTO92	360MW	TA N	30V	TI	TIS 74	554000740
Q31-32	TO106	350MW	TA N	35V	SILICONIX	E111	554000002
Q33	TO-92	350MW	TA NPN	25V	MOTOROLA	MPS6515	550065150
Q34	TO-92	350MW	TA PNP	40V	MOTOROLA	MPS6518	550065180
Q35	MODTO92	360MW	TA N	30V	TI	TIS 74	554000740
Q40	TO-92	350MW	TA NPN	25V	MOTOROLA	MPS6515	550065150
Q41	TO-92	350MW	TA PNP	40V	MOTOROLA	MPS6518	550065180
Q42	TO-5	1W	TA NPN	65V	RCA	2N2102	550021020
Q43	TO-92	350MW	TA NPN	40V	MOTOROLA	2N3903	550039030
Q44	TO5	7W	TA PNP	65V	RCA	2N4036	552040360
Q45	TO92	350MW	TC PNP	40V	MOTOROLA	2N3905	552039050
R2	316-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220231601
R4	301K	1/8W	1%		VARIOUS	RN55 SIZE 50*PPM	222030131
R5	36.5K	1/8W	.1%		VPR	RN55 SIZE 25 PPM	221036529
R6	118K	1/8W	1%		VARIOUS	RN55 SIZE 50*PPM	222011831
R7	13.7K	1/8W	.1%		VPR	RN55 SIZE 25 PPM	221013729
R8	90.9K	1/8W	1%		VARIOUS	RN55 SIZE 50*PPM	222090921
R9	3.74K	1/8W	.1%		VPR	RN55 SIZE 25 PPM	221037419
R10	158K	1/8W	1%		VARIOUS	RN55 SIZE 50*PPM	222015831
R11	1.1K	1/8W	.1%		VPR	RN55 SIZE 25 PPM	221011019
R12	16.5K	1/8W	1%		VARIOUS	RN55 SIZE 50*PPM	222016521
R13	348-	1/8W	.1%		VPR	RN55 SIZE 25 PPM	221034809
R14	4.32K	1/8W	1%		VARIOUS	RN55 SIZE 50*PPM	222043211
R15	110-	1/8W	.1%		VPR	RN55 SIZE 25 PPM	221011009
R16	6.19K	1/8W	1%		VARIOUS	RN55C6191F	222061911
R17	49.9-	1/8W	.1%		VPR	RN55 SIZE 25 PPM	221049999
R18-24	1M	1/4W	10%		AB	TYPE CB	200101056
R25-31	100K	1/4W	10%		AB	TYPE CB	200101046
R32	4.7K	1/4W	10%		AB	TYPE CB	200104726
R33	47K	1/4W	10%		AB	TYPE CB	200104736
R34-41	100K	1/4W	10%		AB	TYPE CB	200101046
R42	100K	1/8W	.1%		VPR	RN55 SIZE 25 PPM	221010039
R43	75K	1/8W	1%		VPR	RN55 SIZE 25 PPM	221075021
R44	31.6K	1/8W	1%		VPR	RN55 SIZE 25 PPM	221031621
R45	22.1K	1/8W	1%		VPR	RN55 SIZE 25 PPM	221022121
R46	3150-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220231611
R47	100K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210031
R48	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R49	147K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220214731
R50	47K	1/4W	10%		AB	TYPE CB	200104736
R51-52	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R53	1.2K	1/4W	10%		AB	TYPE CB	200101226
R54-55	22-	1/4W	10%		AB	TYPE CB	200102206
R56-57	604-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220260401
R58	100K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210031
R59	3.57K	1/8W	1%		VPR	RN55 SIZE 25 PPM	221035711
R60	5.23K	1/8W	1%		VPR	RN55 SIZE 25 PPM	221052311
R61	9.76K	1/8W	1%		VPR	RN55 SIZE 25 PPM	221097511
R62	34.8K	1/8 W	1%		VPR	RN55 SIZE 25 PPM	221034821
R63	56-	1/4W	10%		AB	TYPE CB	200105606
R64	1K	1/4W	10%		AB	TYPE CB	200101026

Table 8—7. (Cont'd).

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
R65	SEL.VAL.	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220200000
R66	7.32K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220273211
R67	8660-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220286611
R68	3090-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220230911
R69	21K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220221021
R70-71	13.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220213721
R72	27.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220227421
R73	4990-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249911
R74	200-	1/2W	10%	200V	HELIPOT	72PMR200	232702013
R75	4990-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249911
R76	40.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220240221
R77	69.8K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220269821
R78-79	20K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220021
R80	8.06K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220280611
R81	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R82	11.5K	1/8W	1%		VARIOUS	RN55C1152F	222011521
R83	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R84	61.9K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220261921
R85	33.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220233221
R86	13K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220213021
R87	16.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220216221
R88	8.06K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220280611
R89	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R90	14.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220214721
R91	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R92	4420-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220244211
R93	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R94	2550-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220225511
R95	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R96	2050-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220511
R97	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R98	4320-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220243211
R99	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R100	698-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220269801
R101-102	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R103	422-	1/8W	1%		VPR	RN55 SIZE 25 PPM	221042201
R104	30.9K	1/8W	1%		VPR	RN55 SIZE 25 PPM	221030921
R105	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R106	215-	1/8W	1%		VPR	RN55 SIZE 25 PPM	221021501
R107	11K	1/8W	1%		VPR	RN55 SIZE 25 PPM	221011021
R108	100K	1/8W	1%		VPR	RN55 SIZE 25 PPM	221010031
R109	5.62K	1/8W	1%		VPR	RN55 SIZE 25 PPM	221056211
R110	432	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220243201
R111	69.8K	1/8W	1%		VPR	RN55 SIZE 25 PPM	221069821
R112	35.7K	1/8 W	1%		VPR	RN55 SIZE 25 PPM	221035721
R113	20K	1/2W	10%	200V	HELIPOT	66WR20K	232702030
R114	41.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220241221
R115	20K	1/2W	10%	200V	HELIPOT	66WR20K	232702030
R116	133-	1/8W	1%		VPR	RN55 SIZE 25 PPM	221013300
R117	1.47K	1/8W	1%		VPR	RN55 SIZE 25 PPM	221014711
R118	1210-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220212111
R119	4.99K	1/8W	1%		VPR	RN55 SIZE 25 PPM	221049911
R120	9.09K	1/8W	1%		VPR	RN55 SIZE 25 PPM	221090911

Table 8—7. (Cont'd).

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
R121-122	10K	1/8W	1%		IRC	RN55 SIZE 25 PPM	221010021
R123-124	20K	1/8W	1%		VPR	RN55 SIZE 25 PPM	221020021
R125	4640-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220246411
R126	20K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220021
R127	191K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220219131
R128	19.1K	1/8W	1%		VPR	RN55 SIZE 25 PPM	221019121
R129	5K	1/2W	10%	200V	HELIPOT	66WR5K	232705021
R130	19.1K	1/8W	1%		VPR	RN55 SIZE 25 PPM	221019121
R131	11.5K	1/8W	1%		VARIOUS	RN55C1152F	222011521
R132	200K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220031
R133	100K	1/2W	10%		HELIPOT	66WR100K	232701042
R134-135	200K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220031
R136-137	200K	1/8W	1%		VPR	RN55 SIZE 25 PPM	221020031
R138	100K	1/2W	10%		HELIPOT	66WR100K	232701042
R139	200K	1/8W	1%		VPR	RN55 SIZE 25 PPM	221020031
R140	100-	1/2	10%		HELIPOT	66WR100	232701012
R141	2K	1/2W	10%	200V	HELIPOT	72PMR2K	232702020
R142	1.78K	1/8W	1%		VPR	RN55 SIZE 25 PPM	221017811
R143	5K	1/2W	10%	200V	HELIPOT	72PMR5K	232705023
R144	10.2K	1/8 W	1%		VPR	RN55 SIZE 25 PPM	221010221
R145	4.12K	1/8W	1%		VPR	RN55 SIZE 25 PPM	221041211
R146	20K	1/2W	10%	200V	HELIPOT	72PMR20K	232702032
R147-148	12K	1/4W	10%		AB	TYPE CB	200101235
R149	SEL.VAL.	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220200000
R150	825-	1/8W	1%		VARIOUS	RN55C8250F	222082501
R151	56-	1/4W	10%		AB	TYPE CB	200105605
R152-154	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R155	130K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220213031
R156	49.9K	1/8W	1%		VARIOUS	RN55C4992F	222049921
R157	16.2K	1/8W	1%		VARIOUS	RN55C1622F	222016221
R158	5K	.75W	10		HELIPOT	89PR5K	232505020
R159	100K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210031
R160	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R161	200K	.75W	10%		HELIPOT	89PR200K	232502040
R162	200K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220031
R163	2.2K	1/4W	10%		AB	TYPE CB	200102226
R164	1K	1/4W	10%		AB	TYPE CB	200101026
R165	2430-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220224311
R166	2K	.75W	10%		HELIPOT	89PR2K	232502020
R167	150K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220215031
R168	100K	1/2W	10%	200V	HELIPOT	72 PMR100K	232701040
R169	4990-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249911
R170	10K	.75W	10%		HELIPOT	89PR10K	232501030
R171	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R172	4990-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249911
R173	118-	1/8W	1%		VARIOUS	RN55 SIZE 100PPM	220211801
R174	9750-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220297611
R175	237-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220223701
R176	24.3K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220224321
R177	365-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220236501
R178	20.5K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220521
R179	499-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249901
R180	45.3K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220245321

Table 8—7. (Cont'd).

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
R181	665-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220266501
R182	28.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220228721
R183	845-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220284501
R184	604K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220260431
R185	1150-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220211511
R186	332K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220233231
R187	1000-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210011
R188	4990-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249911
R189	10K	.75W	10%		HELIPOT	89PR10K	232501030
R190	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R191	4990-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249911
R192	118-	1/8W	1%		VARIOUS	RN55 SIZE 100PPM	220211801
R193	9750-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220297611
R194	237-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220223701
R195	24.3K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220224321
R196	365-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220236501
R197	20.5K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220521
R198	499-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249901
R199	45.3K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220245321
R200	665-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220266501
R201	28.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220228721
R202	845-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220284501
R203	604K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220260431
R204	1150-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220211511
R205	332K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220233231
R206	1000-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210011
R207	348-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220234801
R208	23.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220223221
R209	1780-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220217811
R210	SEL.VAL.	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220200000
R211	3.65K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220236511
R212	280K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220228031
R213	6340-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220263411
R214	182K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220218231
R215	9750-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220297611
R216	422K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220242231
R217	14.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220214721
R218	619K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220261931
R219	10K	1/2W	10%	200V	HELIPOT	72PMR10K	232701030
R220	24.98K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220224921
R221	365K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220236531
R222	11K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220211021
R223-227	20K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220021
R228	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R229	SEL.VAL.	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220200000
R230	20K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220021
R231	3480-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220234811
R232	SEL.VAL.	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220200000
R233	196K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220219631
R234	63.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220263421
R235	1100-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220211011
R236	19.6K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220219621
R237	348-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220234801

Table 8—7. (Cont'd).

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
R238	158-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220215801
R239	1.8K	1/4W	10%		AB	TYPE CB	200101826
R240-241	47-	1/4W	10%		AB	TYPE CB	200104706
R242	7500-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220275011
R243	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R244	13K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220213021
R245	1430-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220214311
R246	51.1-	1/2W	1%		ELECTRA	RN65 SIZE 100 PPM	220651191
R247	511-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220251101
R248	57.6-	1/2W	1%		ELECTRA	RN65 SIZE 100 PPM	220657691
R249	24.9-	1/2W	1%		ECTRA	RN65 SIZE 100 PPM EL	220624991
R250	10-	1/2W	1%		ELECTRA	RN65 SIZE 100 PPM	220610091
R251	SEL.VAL	1/2W	1%		ELECTRA	RN60 SIZE 100 PPM	220600000
R252	SEL.VAL.	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220200000
R253	825-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220282501
R254-255	20K	1/8W	1%		VARIOUS	RN55C2002F	220220021
R256	12-	1/4W	10%		AB	TYPE CB	200101206
R257	1650-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220216511
R258	2870-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220228711
R259-260	1.1K	1/8W	.1%		VPR	RN55 SIZE 25 PPM	221011019
R261	12-	1/4W	10%		AB	TYPE CB	200101205
R262	33K	1/4W	10%		AB	TYPE CB	200103336
R263-264	47-	1/4W	10%		AB	TYPE CB	200104705
R265	500-	1/2W	10%	200V	HELIPOT	72PMR500	232705010
R266-268	1K	1/4W	10%		AB	TYPE CB	200101026
R269	68-	1/4W	10%		AB	TYPE CB	200106806
R270	47-	1/4W	10%		AB	TYPE CB	200104706
R271	68-	1/4W	10%		AB	TYPE CB	200106806
R272	47-	1/4W	10%		AB	TYPE CB	200104705
R273	12-	1/4W	10%		AB	TYPE CB	200101206
R274	47-	1/4W	10%		AB	TYPE CB	200104706
R275	22-	1/4W	10%		AB	TYPE CB	200102205
R276-277	47-	1/4W	10%		AB	TYPE CB	200104706
R278	4020-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220240211
R279	750-	1/8W	1%		VPR	RN55 SIZE 25 PPM	221075001
R280	14K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220214021
R281	SEL.VAL.	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220200000
R282	6190-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220261911
R283	1K	1/4W	10%		AB	TYPE CB	200101026
RT1	RO 10 OHMS AT 25 DEG				FENWAL	KD11J1	290101021
S5	PC BD MTG 3D-1CKT-6POS			NS	OAK	5-22851-734	625000304
S6	SWITCH.PC MTG				CENTRALAB	PX160-280	625000415
S9	PC BD MTG 6D-2CKT-5POS			NS	OAK	5-42621-728	625000301
S10	PC BD MTG 2D-2CKT-5POS			NS	OAK	5-24741-779	625000300
U1	8PDIL			22V	SIGNETICS	NE531	500005310
U2	8PDIL	80MW		180V	NAT.SEMI	LM1458N	500001458
U3	8PDIL				NAT. SEMI	LM741CN	500007412
U4	8PDIL			22V	SIGNETICS	NE531	500005310
U5-6	8PDIL	80MW		180V	NAT.SEMI	LM1458N	500001458
U7	OP.AMP	7295705CM8			NATIONAL	LM318N	500000318

Table 8—7. (Cont'd).

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
U8-10	TO-99				ANALOG	AD518JH	500005180
U11	10P TO-5				RCA	CA3019T	500030190
U12	8P TO99				FAIRCHILD	UA741EHC	500007414
U20	TO-99				ANALOG	AD518JH	500005180
U21	8PDIP			36V	TI	LM311P(SN72311P)	500003111
U22-23	16DIP-P	B		CMOS	RCA	CD4049	510004049
U24-25	8PDIL				NAT. SEMI	LM741CN	500007412
U26-28	8PDIL			22V	SIGNETICS	NE531	500005310
U29-30	8P TO99				ANALOG DEV	AD741J	500007416
VR1	D07	.25W	5%	6.2V	DICKSON	1N823	563008230
W1-2	SHIELDED CABLE						A004400039

Table 8—8. Input/Output Board (A5) Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C7-10	100UF			150V	TSI	PA100PV150N?	301301072
C11	SEL.VAL.				ELMENCO	SEL.VAL.	335400000
C12-13	390 PF		2%	500V	ELMENCO	CM04DD391G0	335403910
C14	.002UF		10%	100V	SPRAGUE	225P20291WD3	320002020
C15	SELVAL		10%		SPRAGUE	225P	320000000
C16	SEL.VAL.				ELMENCO	SEL.VAL.	335400000
E2	PROTECTOR S/V GAS				SIEMENS	B1-C90/20	566009020
R9	855-	1/8W	.1%		VPR	RN55 SIZE 25 PPM	221086609
R10	SEL.VAL.	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220200000
R13	75K	1/2W	1%		ELECTRA	RN65 SIZE 100 PPM	220675021
R14	SEL.VAL.	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220200000
R15-16	69.8-	.75W 70C	1%		TRW ONLY	TO-60	221469891
R17-18	2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220011
R19-20	316-	.75W 70C	1%		TRW ONLY	TO-60	221431601
R21-22	8450-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220284511
R23-24	464-	.75W 70C	1%		TRW ONLY	TO-60	221446401
R25-28	49.9K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249921
R29	1.82K	1/2W	1%		ELECTRA	RN65 SIZE 100 PPM	220618211
R30	22.6K	1/2W	1%		ELECTRA	RN65 SIZE 100 PPM	220622691
R31	340-	1/2W	1%		ELECTRA	RN65 SIZE 100 PPM	220634001
R36	180-	1/4W	10%		AB	TYPE CB	200101916
R37	SEL.VAL.	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220200000
S7	SWITCH,PC MTG				CENTRALAB	PA162-009	625000419
A1	96674 I/O BD A1						A400200018
S8	STRAPPING ASSY S8						A004400042
T1	P50 S900,SPLT TRANS.				UTC	A-20	400200101
T2	LINE TO HI IMP.XFORMER				JAMES	4556	400200300

Table 8—9. Power Tray Assembly Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
A1	96679 PWR SUPPLY A2A1						A004400025
F4-5		.3A		250V	BUSSMAN	MDL	863101500
J12	3-PIN	6A		250V	BELDEN	17252	652201700
J15	4 CKT				BURNDY	MS3112-E-8-4S	654300001
MP1	SHIELD, PLEXIGLASS						A400200106
Q1-2	MODTO220	30W TC NPN		60V	TI	TIP29A	552000291
Q3	MODTO220	40W TC PNP		60V	TI	TIP32A	552000321
S15		3A		125V	SWCRFT	46206LF	645500200
T1		191A			PROFILE	2020	420100101
VR1	TO-3			-12V	NATIONAL	LM320KC-12	500003202
VR2	TO-3			12V	FAIRCHILD	7812KC	500078120
VR3	TO-3			5V	FAIRCHILD	7805KC	500078051
XF4-5	FUSEHOLDER,3AG PANEL				BUSSMAN	HKP	863000100

Table 8—10. Power Supply Board (A2A1) Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1-2	1100UF			30V	SPRAGUE	39D118G030GP4	300001180
C1-2	1100UF			30V	SPRAGUE	39D118G030GP4	300001180
C3	4000UF			25V	SPRAGUE	39D408G025JS4	300004080
C3	4000UF			25V	SPRAGUE	39D408G025JS4	300004080
C4-6	4.7UF		10%	50V	KEMET	T330C475K050AS	310004750
C4-6	4.7UF		10%	50V	KEMET	T330C475K050AS	310004750
C7-9	22UF	B	10%	15V	SPRAGUE	196D226X9015KA1	310802263
C7-9	22UF	B	10%	15V	SPRAGUE	196D226X9015KA1	310802263
C10-12	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
C10-12	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
C13	200UF			25V	MALLORY	MTV200DE25	301402072
C13	200UF			25V	MALLORY	MTV200DE25	301402072
CR1-17	DO41	1A	SI	200V	EDAL	1N4003	560040030
CR1-17	DO41	1A	SI	200V	EDAL	1N4003	560040030
CR18	DO35 4NS 10MA		SI	50UA	FAIRCHILD	IN4148	560041480
CR18	DO35 4NS 10MA		SI	50UA	FAIRCHILD	IN4148	560041480
CR19-21	DO41	1A	SI	200V	EDAL	1N4003	560040030
CR19-21	DO41	1A	SI	200V	EDAL	1N4003	560040030
E29-30	TERMINAL,FK TURRET,SWAGE				CAMBION	140-1784-02-01-00	838001402
E29-30	TERMINAL,FK TURRET,SWAGE				CAMBION	140-1784-02-01-00	838001402
F1-3		2A		250V	LITTELFUSE	3AG	863100600
F1-3		2A		250V	LITTELFUSE	3AG	863100600
J1	16 COND				AMP	350214-1	650900900
J1	16 COND				AMP	350214-1	650900900
K1	RELAY,4C-PC M/O-14V				MIDTEX	156-24C-1A9	604102500
K1	RELAY,4C-PC M/O-14V				MIDTEX	156-24C-1A9	604102500
K2	2 VOLT D.O.MAX.			24V	MIDTEX	156-24C1B4	604100701
K2	2 VOLT D.O.MAX.			24V	MIDTEX	156-24C1B4	604100701

Table 8—10. (Cont'd).

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
Q1	TO-92	350MW	TA	NPN 40V	MOTOROLA	2N3903	550039030
Q1	TO-92	350MW	TA	NPN 40V	MOTOROLA	2N3903	550039030
Q2	TO92	350MW	TC	PNP 40V	MOTOROLA	2N3905	552039050
Q2	TO92	350MW	TC	PNP 40V	MOTOROLA	2N3905	552039050
Q3	TO-92	350MW	TA	NPN 40V	MOTOROLA	2N3903	550039030
Q3	TO-92	350MW	TA	NPN 40V	MOTOROLA	2N3903	550039030
Q4-5	TO92	350MW	TC	PNP 40V	MOTOROLA	2N3905	552039050
Q4-5	TO92	350MW	TC	PNP 40V	MOTOROLA	2N3905	552039050
Q6	TO-92	350MW	TA	NPN 25V	MOTOROLA	MPS6515	550065150
Q6	TO-92	350MW	TA	NPN 25V	MOTOROLA	MPS6515	550065150
Q7-8	TO92	350MW	TC	PNP 40V	MOTOROLA	2N3905	552039050
Q7-8	TO92	350MW	TC	PNP 40V	MOTOROLA	2N3905	552039050
Q9	TO-92	350MW	TA	NPN 25V	MOTOROLA	MPS6515	550065150
Q9	TO-92	350MW	TA	NPN 25V	MOTOROLA	MPS6515	550065150
R1	4-	3W	5%		W.LEONARD	TYPE 3X	210304095
R1	4-	3W	5%		W.LEONARD	TYPE 3X	210304095
R2	1.96K	1/8W	.5%		ELECTRA	RN55 SIZE 100 PPM	220319617
R2	1.96K	1/8W	.5%		ELECTRA	RN55 SIZE 100 PPM	220319617
R3	1K	1/8W	.5%		ELECTRA	RN55 SIZE 100 PPM	220310017
R3	1K	1/8W	.5%		ELECTRA	RN55 SIZE 100 PPM	220310017
R4	4-	3W	5%		W.LEONARD	TYPE 3X	210304095
R4	4-	3W	5%		W.LEONARD	TYPE 3X	210304095
R5	1.96K	1/8W	.5%		ELECTRA	RN55 SIZE 100 PPM	220319617
R5	1.96K	1/8W	.5%		ELECTRA	RN55 SIZE 100 PPM	220319617
R6	1K	1/8W	.5%		ELECTRA	RN55 SIZE 100 PPM	220310017
R6	1K	1/8W	.5%		ELECTRA	RN55 SIZE 100 PPM	220310017
R7	2-	2W	5%		IRC	BWH	210202095
R7	2-	2W	5%		IRC	BWH	210202095
R8	523-	1/8W	.5%		ELECTRA	RN55 SIZE 100 PPM	220352307
R8	523-	1/8W	.5%		ELECTRA	RN55 SIZE 100 PPM	220352307
R9	1K	1/8W	.5%		ELECTRA	RN55 SIZE 100 PPM	220310017
R9	1K	1/8W	.5%		ELECTRA	RN55 SIZE 100 PPM	220310017
R10	39-	1/4W	10%		AB	TYPE CB	200103906
R10	39-	1/4W	10%		AB	TYPE CB	200103906
R11	2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220011
R11	2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220011
R12-13	100K	1/4W	10%		AB	TYPE CB	200101046
R12-13	100K	1/4W	10%		AB	TYPE CB	200101046
R14	820K	1/4W	10%		AB	TYPE CB	200108246
R14	820K	1/4W	10%		AB	TYPE CB	200108246
R15	28K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220228021
R15	28K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220228021
R16-17	57.6K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220257621
R16-17	57.6K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220257621
R18	220K	1/4W	10%		AB	TYPE CB	200102246
R18	220K	1/4W	10%		AB	TYPE CB	200102246
R19	100K	1/4W	10%		AB	TYPE CB	200101046
R19	100K	1/4W	10%		AB	TYPE CB	200101046
R20-22	22.6K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220222621
R20-22	22.6K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220222621
R23	1K	1/8W	.5%		ELECTRA	RN55 SIZE 100 PPM	220310017
R23	1K	1/8W	.5%		ELECTRA	RN55 SIZE 100 PPM	220310017
R24	1820-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220218211
R24	1820-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220218211
U1-3	8PDIL				NAT. SEMI	LM741CN	500007412
U1-3	8PDIL				NAT. SEMI	LM741CN	500007412
XF1-3	FUSECLIP,PC MTG,FUSE STOP				LITTLEFUSE	102068	863300301
XF1-3	FUSECLIP,PC MTG,FUSE STOP				LITTLEFUSE	102068	863300301

Table 8—11. Digital Board (A3) Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1	8-35PF			200V	ERIE	539-002D-8-35	340103500
C2	SEL.VAL.				ELMENCO	SEL.VAL.	335400000
C3	47PF		5%	100V	ELMENCO	CM04-A470J0-	335404700
C4	100PF		2%	500V	ARCO	CM04FD101GD	335401010
C5	130PF		5%	100V	ELMENCO	CM04-A131J0-	335401310
C6	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
C7	.1UF		10%	100V	SPRAGUE	225P10491WD3	320001040
C8-9	47PF DA N330		10%	1KV	CENTRALAB	DD-470	330004700
C10	10000PF		2%	500V	ELMENCO	CM07FD103G03	335401030
C11-13	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
C14	.0027UF		10%	100V	SPRAGUE	225P27291WD3	320002720
C15	.018UF		10%	100V	SPRAGUE	225P18391WD3	320001830
C16	.082UF		10%	100V	SPRAGUE	225P82391WD3	320008230
C17	.68UF		10%	100V	PAKTRON	TYPE WC	321906840
C19	330PF		5%	100V	ELMENCO	CM04-A331J0-	335403310
C20	4.7UF		20%	25V	TSI	PA4.7EE25NPT	301304750
C21-24	.1UF		20%	100V	VITRAMON	VK33BW104M	331001040
C25-26	4.7UF		10%	25V	KEMET	T330A475K025AS	310004751
C27-28	22UF		10%	15V	KEMET	T330C226K015AS	310002261
C29-34	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
C35	20UF			16V	SPRAGUE	TE1157	300202060
C36	100UF			25V	SPRAGUE	TE1211	300201073
C37	2.2UF	B	10%	35V	SPRAGUE	196D225X9035JA1	310802250
C38-39	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
CR1	A50X	.5W	SI	175V	TI	IN459A	560004591
CR2-15	DO35 4NS 10MA		SI	50UA	FAIRCHILD	IN4148	560041480
CR16	DO35 4NS 10MA		SI	50UA	TI	1N4152	560041520
CR17-20	DO35 4NS 10MA		SI	50UA	FAIRCHILD	IN4148	560041480
J11-12	SKT IC 16P PC				AUGAT	316-AG5D-2R	820100400
Q1-3	TO-92 350MW TA	NPN		25V	MOTOROLA	MPS6515	550065150
Q4	MODTO92 360MW TA	N		30V	TI	T1S75	554000750
Q5	TO92 350MW TC	PNP		40V	MOTOROLA	2N3905	552039050
Q6-8	TO-92 350MW TA	NPN		25V	MOTOROLA	MPS6515	550065150
Q9	TO92 350MW TC	PNP		25V	MOTOROLA	MPS6519	552065190
R1	215K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220221531
R2	4640-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220246411
R3	6810-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220268111
R4	1K	1/4W	10%		AB	TYPE CB	200101026
R5	10-	1/4W	10%		AB	TYPE CB	200101006
R6	2.2K	1/4W	10%		AB	TYPE CB	200102226
R7-9	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R10-11	10K	1/4W	10%		2	00 A410100315R71-7	200101036
R12	806K	1/8	1%		VPR	VM6-8063FC	222280631
R13	100K	.75W	10%		HELIPOT	89PR100K	232501040
R14	100K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210031
R15-16	100K	1/4W	10%		AB	TYPE CB	200101046
R17	6190-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220261911
R18	10.5K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210521
R19	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R20	1.37K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220213711
R21	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R22	1M	1/4W	10%		AB	TYPE CB	200101056
R23	30.1K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220230121
R24	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R25	5K	1/2W	10%	200V	HELIPOT	66WR5K	232705021
R26	18.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220218221
R27	39K	1/4W	10%		AB	TYPE CB	200103936

Table 8—11. (Cont'd).

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
R28	22K	1/4W	10%		AB	TYPE CB	200102236
R29	10K	1/4W	10%		2	00 A410100015R71-7	200101036
R30	158K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220215831
R31	100K	1/4W	10%		AB	TYPE CB	200101046
R32	22K	1/4W	10%		AB	TYPE CB	200102236
R33	100K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210031
R34	100K	1/4W	10%		AB	TYPE CB	200101046
R35	75K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220275021
R36-37	3.3K	1/4W	10%		AB	TYPE CB	200103326
R38	4990-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249911
R39	30.1K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220230121
R40	4990-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249911
R41-42	4.7K	1/4W	10%		AB	TYPE CB	200104726
R43	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R44-45	22K	1/4W	10%		AB	TYPE CB	200102236
R46	1K	1/4W	10%		AB	TYPE CB	200101026
R47	1.5M	1/4W	10%		AB	TYPE CB	200101556
R48	33K	1/4W	10%		AB	TYPE CB	200103336
R49	133K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220213331
R50	31.6K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220231621
R51	7.32K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220273211
R52	1580-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220215811
R53	1130-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220211311
R54-55	15K	1/4W	10%		AB	TYPE CB	200101536
R56-57	22K	1/4W	10%		AB	TYPE CB	200102236
R58-59	10-	1/4W	10%		AB	TYPE CB	200101006
R60	4.7K	1/4W	10%		AB	TYPE CB	200104726
R61-64	47K	1/4W	10%		AB	TYPE CB	200104736
R65	15K	1/4W	10%		AB	TYPE CB	200101536
R66	33K	1/4W	10%		AB	TYPE CB	200103336
R67	10K	1/4W	10%		2	00 A410100015R71-7	200101036
R68	12.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220212721
R69	49.9K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249921
R70	1000-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210011
R71	100K	1/4W	10%		AB	TYPE CB	200101046
R72	19.6K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220219621
R73	1000-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210011
R74	19.6K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220219621
R75	3.92K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220239211
R76	40.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220240221
R77	84.5-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220284591
R78	1820-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220218211
R79-80	19.6K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220219621
R81	100-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210001
R82	100K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210031
R83	100K	1/2W	10%		HELIPOT	66WR100K	232701042
R84	100K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210031
R85	499-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249901
R86	19.6K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220219621
R87	500-	1/2W	10%	200V	HELIPOT	66WR500	232705011
R88-91	2.2K	1/4W	10%		AB	TYPE CB	200102226
R92	150K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220215031
R93	100K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210031
S11	SWITCH,PB,2POLES,MOMENTRY				SCHADOW	1XF(NONE)FG3LACK2U0A	635800901
S12	SWITCH,PB,4POLES,MOMENTRY				SCHADOW	1XF(NONE)FG3LACK4U0A	635800902
S13	SWITCH,PB,6POLES,MOMENTRY				SCHADOW	1XF(NONE)FG3LACK6U0A	635800903
S14	SWITCH,PB,2POLES,MOMENTRY				SCHADOW	1XF(NONE)FG3LACK2U0A	635800901
U1	14DIP-P	B			CMOS RCA	CD4013	510004013
U2	16DIP-P	B			CMOS RCA	CD4017	510004017
U3	16DIP-P	B			CMOS RCA	CD4020	510004020

Table 8—11. (Cont'd).

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
U4	16DIP-P		B		CMOS RCA	CD4017	510004017
U5	8P TO99				FAIRCHILD	UA741EHC	500007414
U6	8PDIL	80MW		180V	NAT.SEMI	LM1458N	500001458
U7	14DIP-P		B		CMOS RCA	CD4001	510004001
U8	16DIP-P		B		CMOS RCA	CD4049	510004049
U9	14DIP-P		B		CMOS RCA	CD4011	510004011
U10	14DIP-P		B		CMOS RCA	CD4024	510004024
U11-12	14DIP-P		B		CMOS RCA	CD4001	510004001
U13-14	8LEDTO-5				RCA	CA3130S	500031300
U15	14DIP-P		B		CMOS RCA	CD4011	510004011
U16	14DIP-P		B/UB		CMOS RCA	CD4023	510004023
U17	16DIP-P		B		CMOS RCA	CD4029	510004029
U18	16DIP-P		B		CMOS MOTOROLA	MC14028	510004028
U19	14DIP-P		B		CMOS RCA	CD4001	510004001
U20	16DIP-P		B		CMOS RCA	CD4008	510004008
U21	16DIP-P		B		CMOS RCA	CD4019	510004019
U22-23	14DIP-P		B		CMOS RCA	CD4001	510004001
U24-25	14DIP-P		B		CMOS RCA	CD4011	510004011
U26	14DIP-P		B		CMOS RCA	CD4001	510004001
U27	16DIP-P		B		CMOS RCA	CD4049	510004049
U28	8PDIL	80MW		180V	NAT.SEMI	LM1458N	500001458
U29	14DIP-P		B		CMOS RCA	CD4001	510004001
U30	16DIP-P		B		CMOS RCA	CD4029	510004029
U31	14DIP-P		B		CMOS RCA	CD4016	510004016
U32	16DIP-P		B		CMOS MOTOROLA	MC14046	510004046
U33	14DIP-P		B		CMOS RCA	CD4013	510004013
U34	8PDIL				NAT. SEMI	LM741CN	500007412
U35-36	TO-99				ANALOG	AD518JH	500005180
U37	14DIP-P		B		CMOS RCA	CD4001	510004001
U38-42	16DIP-P		B		CMOS RCA	CD4029	510004029
U43	14DIP-P		B		CMOS RCA	CD4001	510004001
U44-47	16DIP-P		B		CMOS RCA	CD4042	510004042
U48-51	14DIP-P		B		CMOS RCA	CD4016	510004016
U52	14DIP-P		B		CMOS RCA	CD4013	510004013
U53	16DIP-P		B		CMOS MOTOROLA	MC14555	510004555
U54	14DIP-P		B		CMOS RCA	CD4001	510004001
U55	16DIP-P		B		CMOS MOTOROLA	MC14015	510004015
U56	14DIP-P		B		CMOS RCA	CD4001	510004001
U57-59	14DIP-P		B		CMOS RCA	CD4011	510004011
U60-61	14DIP-P		B		CMOS RCA	CD4013	510004013
U62-63	14DIP-P		B		CMOS RCA	CD4001	510004001
U64	16DIP-P		B		CMOS RCA	CD4017	510004017
U65	8DIP-P				LM SIGNETICS	NE 555V	510005550
U66	14DIP-P		B		CMOS RCA	CD4013	510004013
U67	14DIP-P		B		CMOS RCA	CD4011	510004011
U68	14DIP-P		B		CMOS RCA	CD4002	510004002
U69-70	14DIP-P		B		CMOS RCA	CD4001	510004001
U71	14DIP-P		B		CMOS RCA	CD4011	510004011
U72	16DIP-P		B		CMOS RCA	CD4050	510004050
U73	8PDIL	80MW		180V	NAT.SEMI	LM1458N	500001458
U74	14DILP				RCA	CA3046	500030460
U75	8P TO99				FAIRCHILD	UA741EHC	500007414
U76	14DIP-P		B		CMOS RCA	CD4001	510004001
XA15	SKT IC 16P PC				AUGAT	316-AG5D-2R	820100400
XY1	SKT				AUGAT	8000-DG3	826500130
Y1	4.096MHZ		005		ERIE	4.096MHZ HC-6/U	919100001

Table 8—12. C-MSG Filter Board (A4A1) Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1-8	.01UF		1%	100V	FDYNE	PPA-11-.01-100-1	322401030
C9-10	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
C11	15PF	DA N330	10%	1KV	CENTRALAB	DD-150	330001500
P1	4 SIP LWR HALF				BERG	65521-104	6540031 32
P2	2 SIP LWR HALF				BERG	65521-102	6540031 34
Q1-2	TO92	350MW	TC	PNP	50V MOTOROLA	2N5087	5520503 70
Q3	TO-92	350MW	TA	NPN	25V MOTOROLA	2N5089	550050890
Q4	TO92	350MW	TC	PNP	50V MOTOROLA	2N5087	5520503 70
Q5-6	TO-92	350MW	TA	NPN	25V MOTOROLA	2N5089	550050890
Q7	TO92	350MW	TC	PNP	50V MOTOROLA	2N5087	5520503 70
Q8	TO-92	350MW	TA	NPN	25V MOTOROLA	2N5089	550050890
R1	14.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220214721
R2	200K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220031
R3	34K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220234021
R4	4220-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220242211
R5	2K	1/2	10%		HELIPOT	72XWR2K	232702027
R6	13.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220213721
R7-8	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R9	23.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220223721
R10	15K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220215021
R11	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R12	8.87K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220288711
R13	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R14	19.1K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220219121
R15	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R16	1.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220214011
R17	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R18	8.87K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220288711
R19	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R20-23	100-	1/4W	10%		AB	TYPE CB	200101016

Table 8—13. Optional Battery Pack Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TCL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
BT1		2.6AH		6V	GLOBE	GC626-18	910000101
BT2-3		1.5AH		12V	GLOBE	GC1215-18	910000102
F1—F3		5A		250V	LITTLEFUSE	3AG	8631009 00

* Batt. Pack (Includes Housing + Cells) — A400200040 (Tan) — 1 ea.

AP 11/15/93

ONE NOTE CAUTION No. Serv. 0

CHANGES HAVE BEEN MADE * ON THIS PAGE. SEE ISSUE SHEET.

CAUTION
CHANGES HAVE BEEN MADE
ON THIS PAGE.
SEE ISSUE SHEET.

SECTION 9

MODEL DIFFERENCES

9.1 Model 4002R Transmission And Impulse Noise Distribution Set

9.2 The Model 4002R Transmission And Impulse Noise Distribution set is the rack mount-version of the portable Model 4002. The rack-mount Model 4002R test set has all the features of the portable series, except for the internal batteries. The rack-mount test set is powered by 115 Vac only. The Model 4002R has an additional set of 310-type jacks which permit use of a 52A headset for signal monitoring. And, the rack mount version has its major front panel connections paralleled to a terminal strip on the rear panel for use in permanent installations.

9.3 Specification Differences

9.4 The Model 4002R test set meet all specifications shown in Table 2—1, except for size, 17 × 6-7/8 × 11-3/4 in (43.2 × 17.5 × 29.8 cm) and weight, approximate 21 lb (9.5 kg). Frequency response information for the bandpass and noise weighting filters are identical to the standard Model 4002 and is shown in Figure 2—1 through 2—6.

9.5 Rack Mounting The Model 4002R

9.6 Refer to Figure 9—1 for installation information on the Model 4002R. Make wiring connections to the rear of the Model 4002R according to the information presented in Figure 9—2 and Table 9—1.

9.7 Controls And Connectors Differences

9.8 Figure 9—2 shows the front and rear panel controls. Table 9—1 is a supplement to Table 4—1 and briefly describes the controls and connectors for the Model 4002R that are different from those of the standard Model 4002.

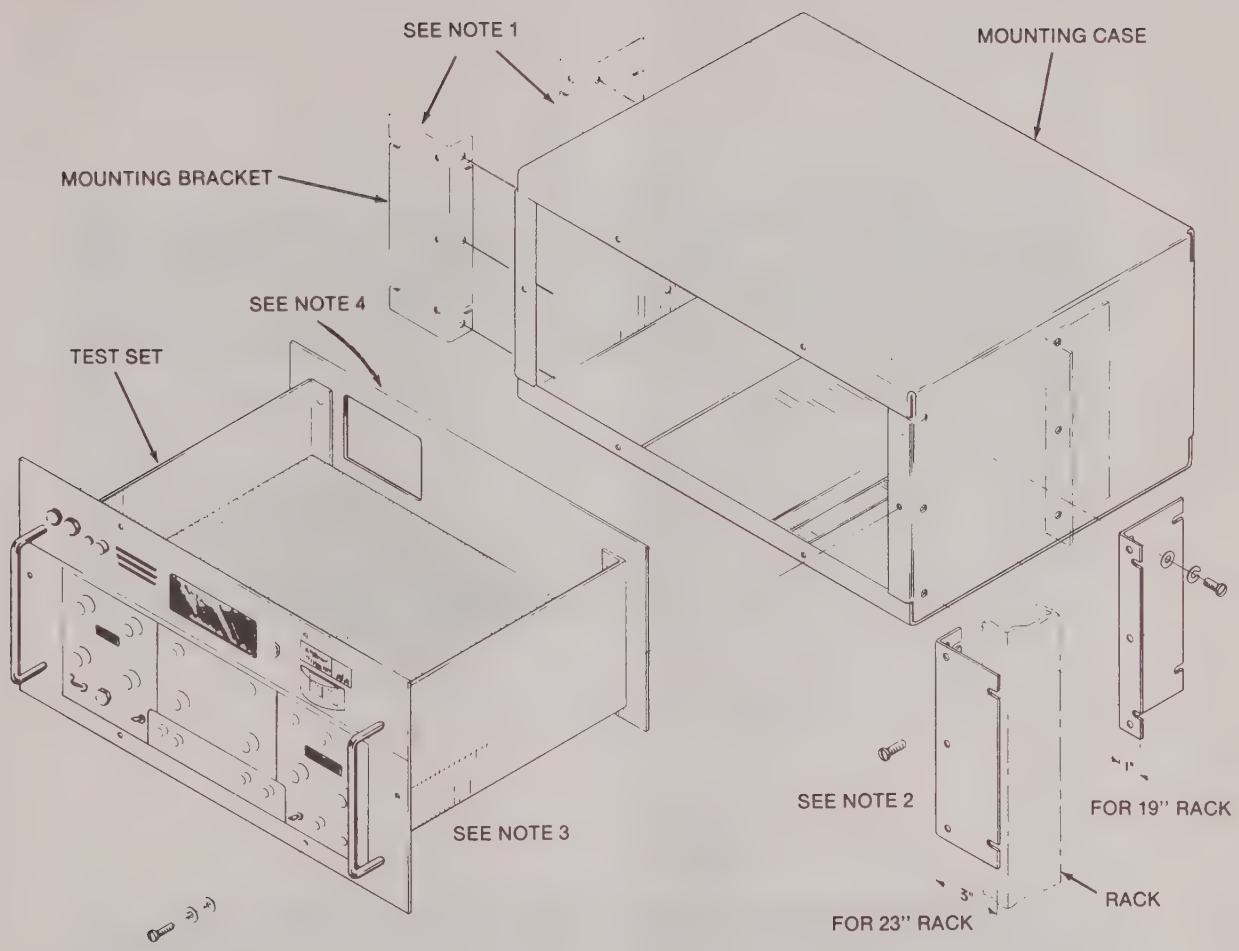
9.9 A Model 44-30 Remote Display is available to extend the Model 4002R digital test result readout to a maximum of three additional locations. Each location can be as far as 250 cable feet (76 meters) from the test set itself.

9.10 Diagrams And Parts List

9.11 Figure 9—3 is a functional diagram of the Model 4002R Input/Output switching section (I/O Impedance Board). Figures 9—4 through 9—7 and Tables 9—2 through 9—4 are assembly diagrams and parts lists for the Model 4002R rack-mounted test set.

Table 9—1. Controls And Connectors.

REFERENCE DESIGNATION	NOMENCLATURE	DESCRIPTION
J2, J3	Line A and B 309-jacks	Enable connection of external circuits to test set.
J10	DIAL 310-jack	Provides a quick and convenient way to connect a lineman's handset for dialing through the test set.
J13, J14	310 T&R, 52A, 310-jacks	Disconnects internal speaker and permits remote monitoring of signals present on a circuit under test. An external listening device may be connected to 310 T&R jack J13. The ring lead carries the signals and the tip is grounded. A 52A headset may be connected to 52A jacks J13 and J14 for listening to signals in a noisy environment.
TB1	terminal block	Enables connecting two circuits under test to the rear panel instead of the front panel jacks.
REMOTE DISPLAY OPTION	REMOTE DISPLAY 50 pin connector	Present only when the remote option board of the Model 44-30 Remote Display is installed in the Model 4002R. Provides a connection to the Model 44-30 Remote Display.
	FREQUENCY RANGING switch	The FREQUENCY RANGING switch is not used in the Model 4002R. The 4002R test set automatically selects the appropriate frequency range when in the frequency measuring mode. Both the test set and the remote display show identical data.



NOTES

1. BRACKETS MAY BE MOUNTED AT THE FRONT OR THE MIDDLE OF THE CASE. SECURE BRACKETS TO CASE WITH 10-32 MACHINE SCREWS, WASHERS, AND LOCK WASHERS.
2. BRACKETS MAY BE USED FOR 19" OR 23" RACKS. SECURE BRACKETS TO A RACK WITH 12-24 MACHINE SCREWS.
3. TEST SET ENTERS THE CASE THROUGH THE FRONT. SECURE TEST SET TO CASE WITH 6-32 MACHINE SCREWS, WASHERS, AND LOCK WASHERS.
4. CONNECT POWER CORD AT REAR OF TEST SET THROUGH OPENING IN THE CASE.
5. SELECT APPROPRIATE FUSE SIZE AND SET 115/230V SWITCH AT CORRECT POSITION FOR AC POWER SOURCE AVAILABLE

Figure 9—1. Rack Mounting The Model 4002R.

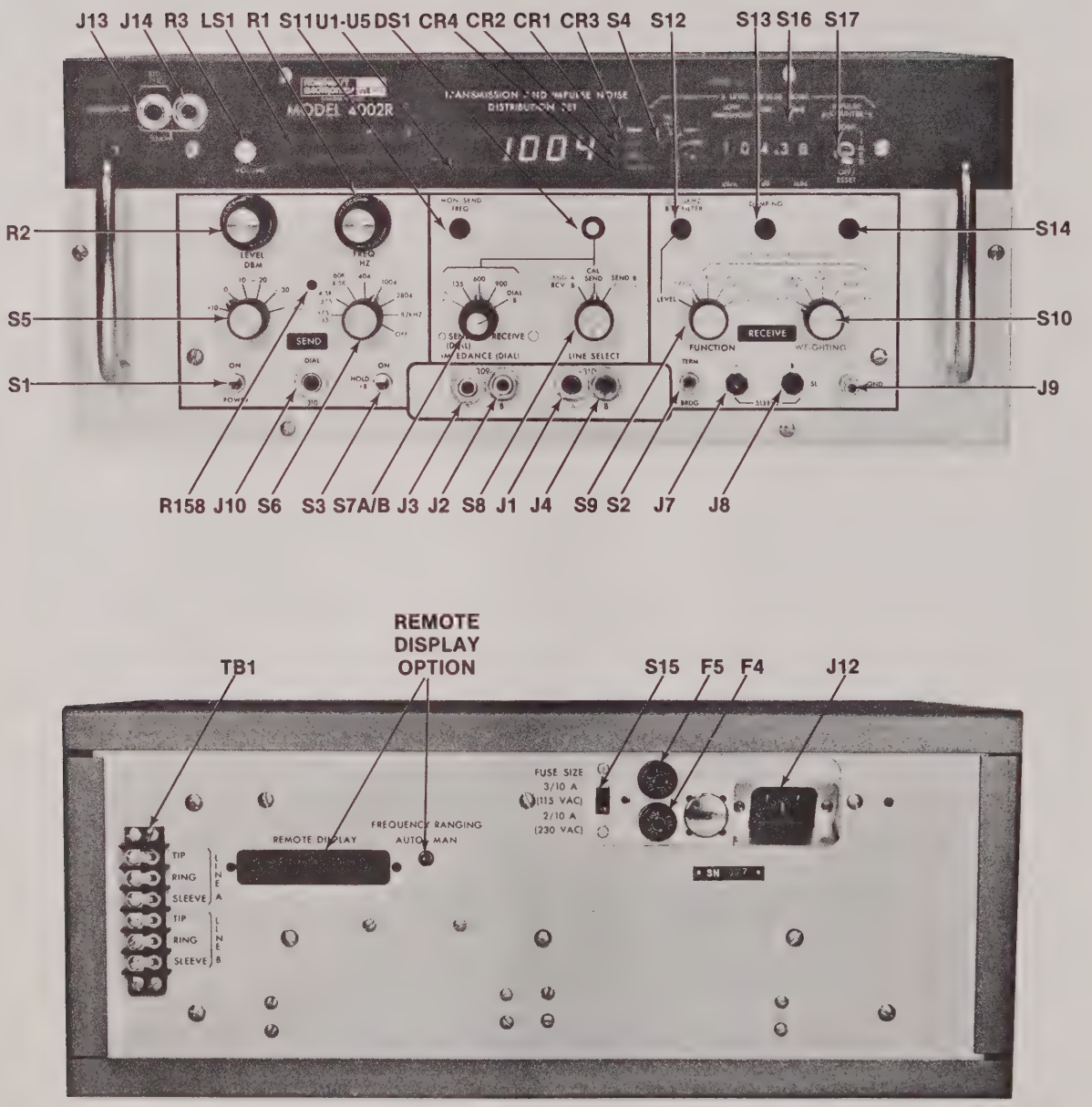


Figure 9—2. Model 4002R Front and Rear Panel Controls.

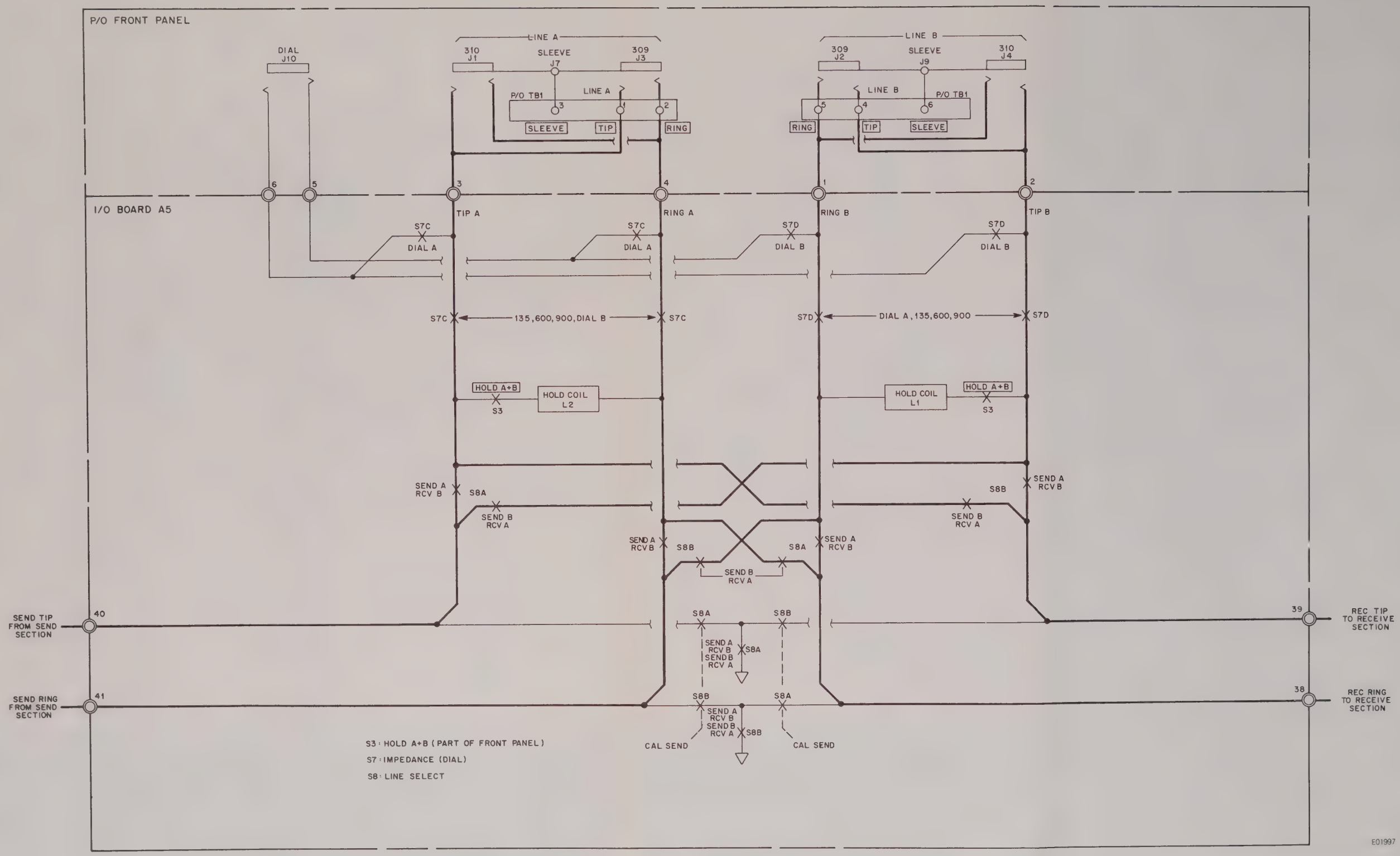
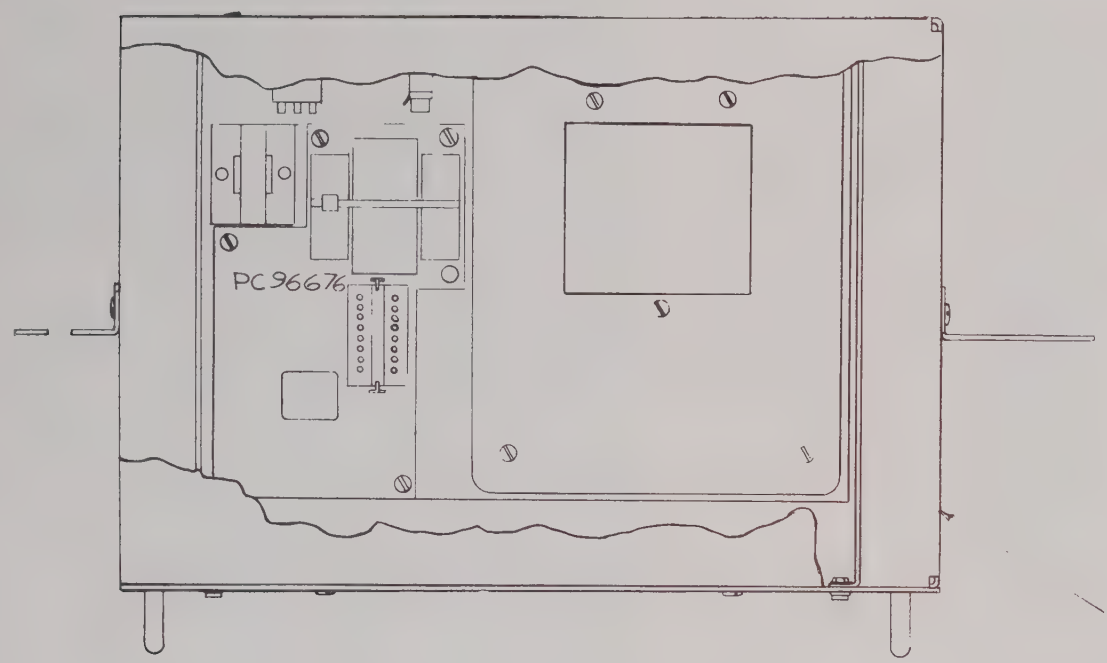
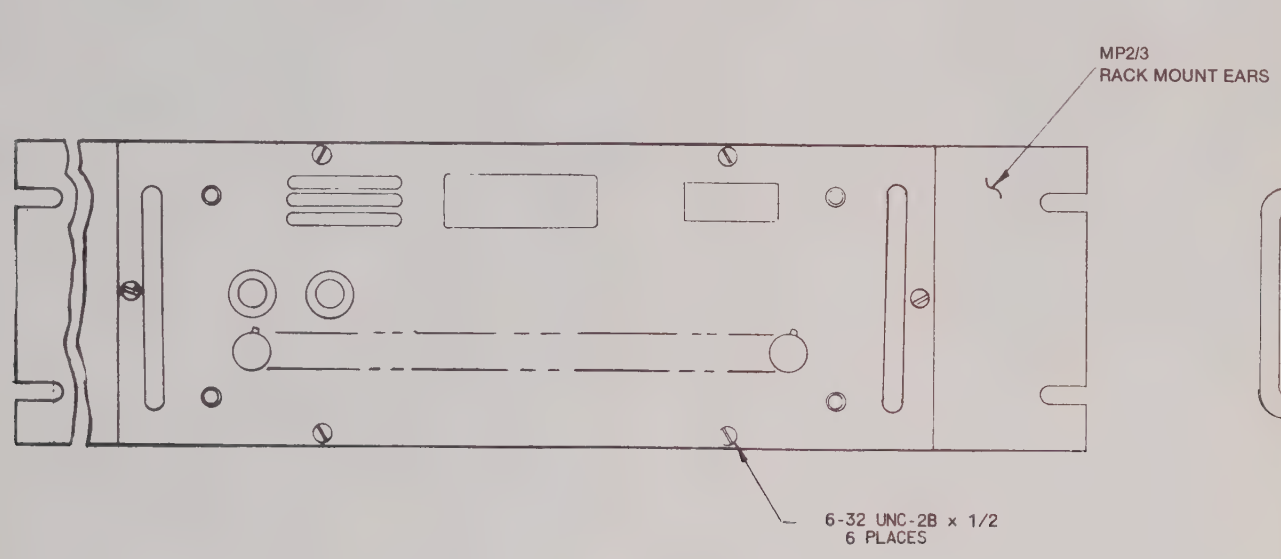
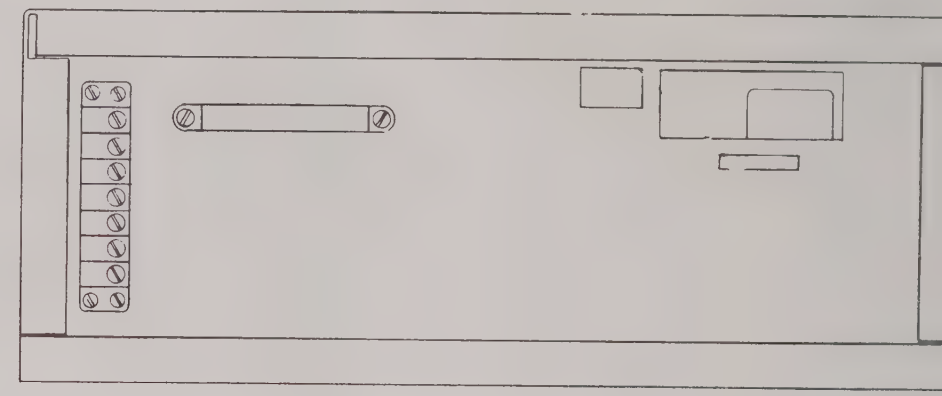


Figure 9—3. Model 4002R Input/Output Switching Section (I/O Impedance Board) Functional Diagram.







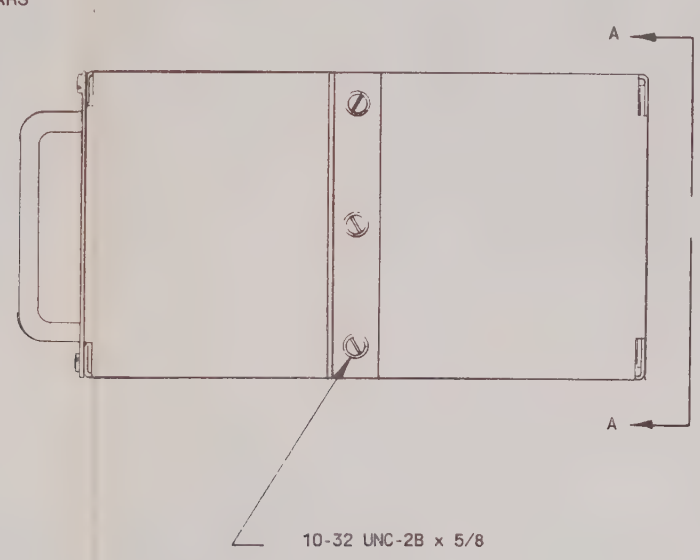
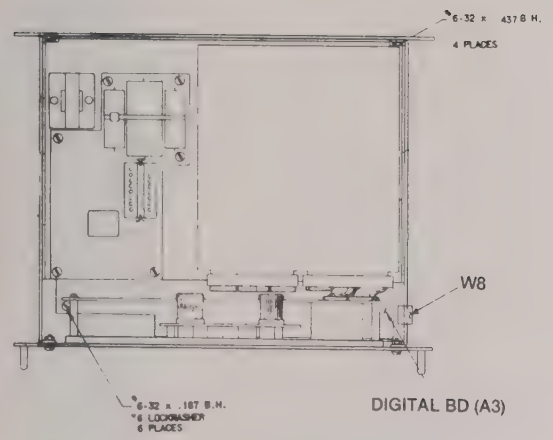
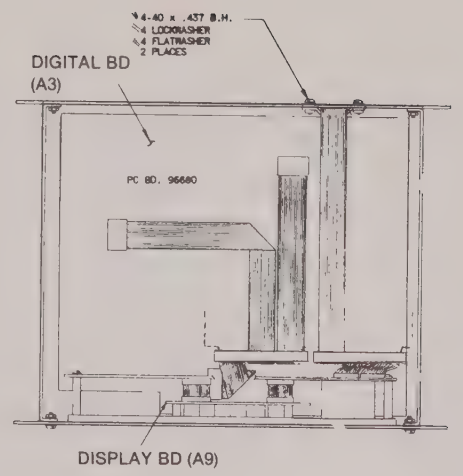
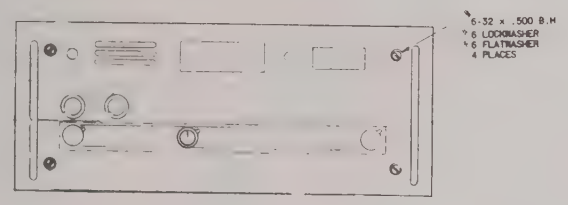
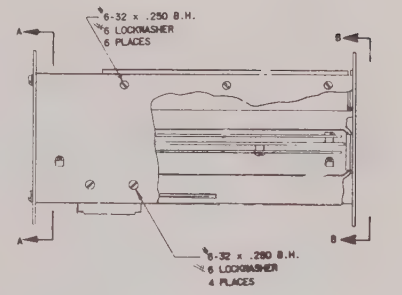


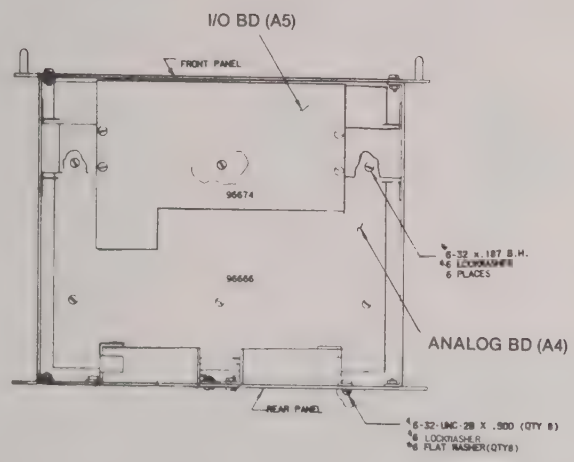
Figure 9—4. Model 4002R Top Unit Assembly Diagram.

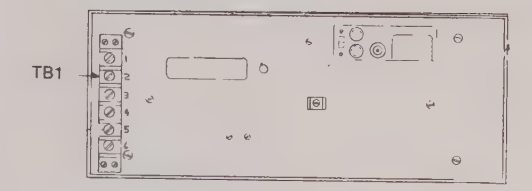


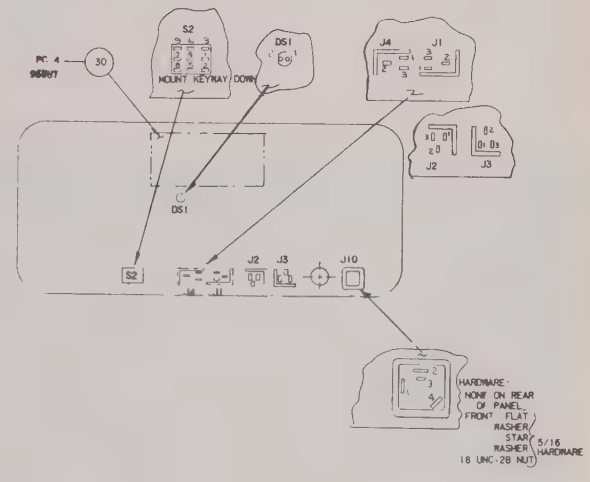












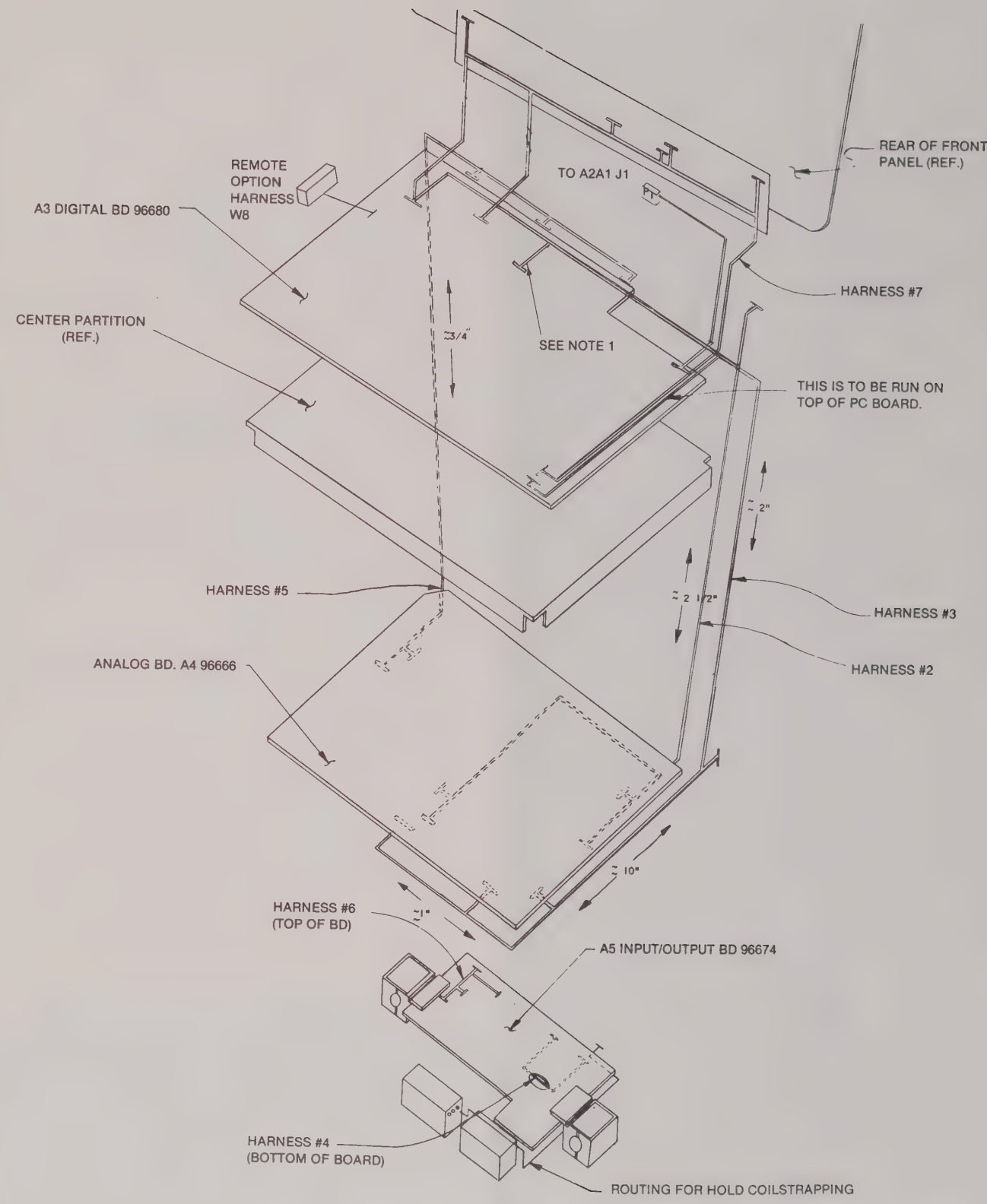


Figure 9—5. Model 4002R Overall Assembly Diagram.

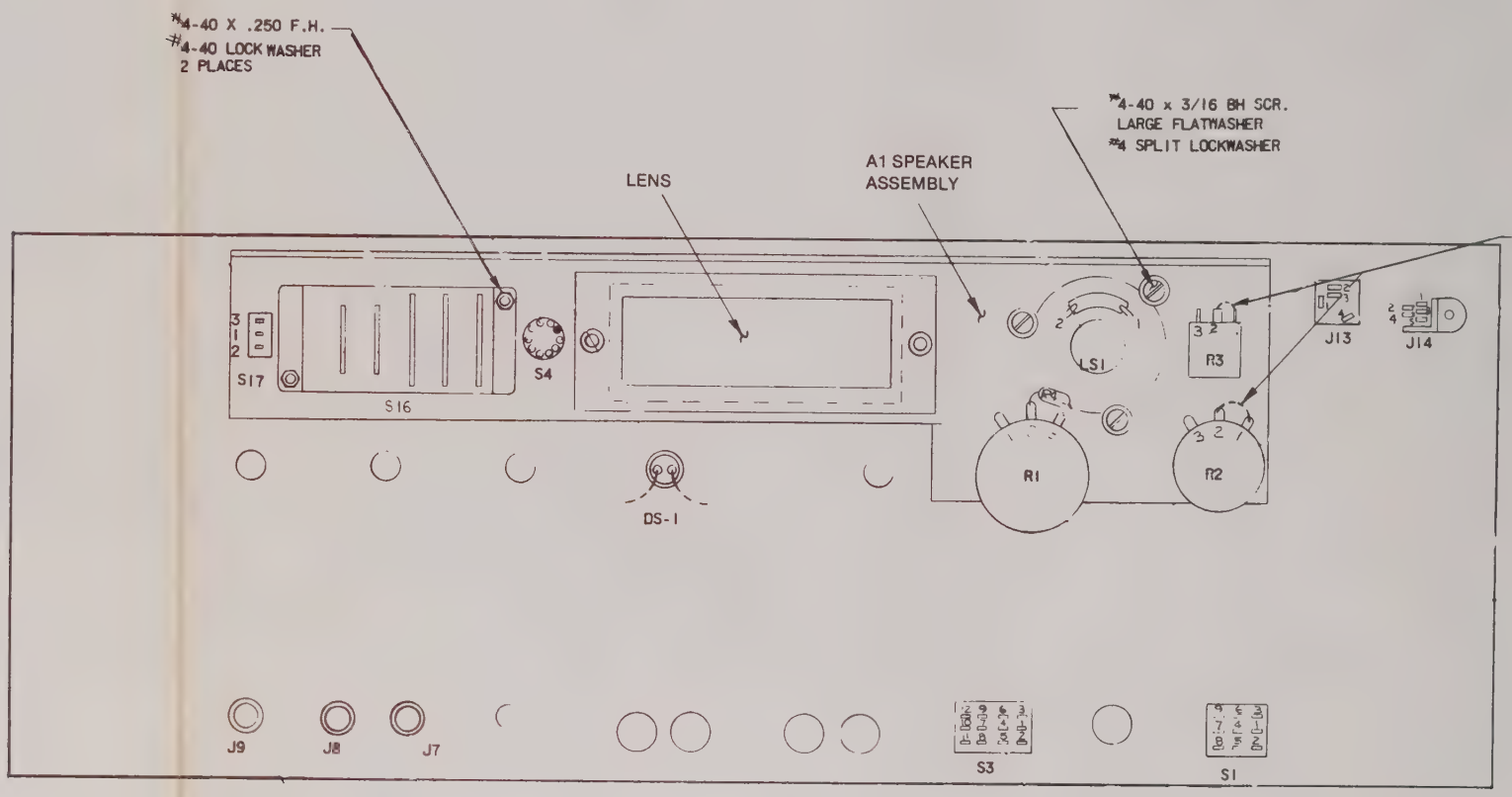


Figure 9—6. Model 4002R Front Panel Assembly Diagram.

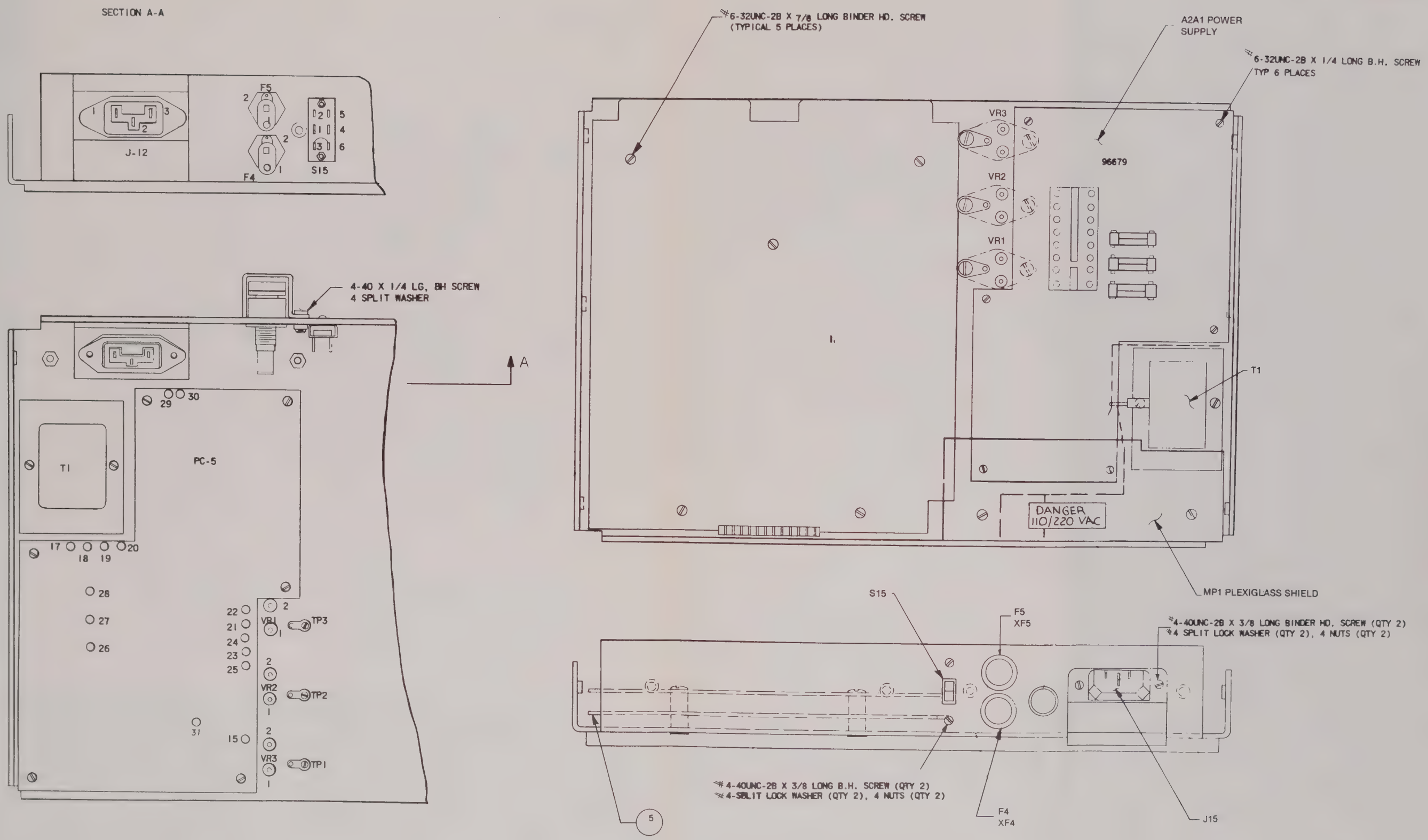


Figure 9—7. Power Supply Assembly Diagram.

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Table 9—2. Model 4002R Overall Assembly Parts List.

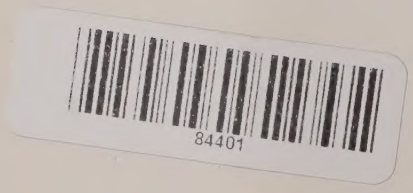
REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
A3	PC 96680 LOGIC BD						A400200025
A4	96666 ANALOG BD A4						A400200017
A5	FINAL I/O BD ASSY A5						A400200024
DS1	W/LEADS	20MA		1.7V	INT-MARKET	L617R-100R	726100001
H4	HARNESS SHEET #4						A004400016
H5	HARNESS SHEET#5						A004400018
H6	HARNESS SHEET #6						A004400037
J1	WIRING ASSY J1,4						A004401043
J2-3	JACK,309,SCHEM 4				TCC	350CTB/S/	650402101
J4	WIRING ASSY J1,4						A004401043
J7-8	BLACK NYLON PHONE				HH SMITH	241	650500100
J9	BINDING POST METAL GND				H H SMITH	137SP	652500100
J10	HI-D				SWCRFT	M-1128	650101300
J13	HI-D				SWCRFT	M-1128	650101300
J14	N/P				SWCRFT	5J-1594	650403200
L1-2	4H				NEWTON	TN-1274	450200200
LS1	8-	.1W			PHILMORE	TS19	926000015
PC4	PC ASSY 96867 DISPLAY BD						A400200013
PC10	PC ASSY 96885 DISPLAY DRV						A400200016
R1	20K	LINEAR	3%		DE YOUNG	MODEL 23A	240102030
R2	10 K	2 W	5%		SPECTROL	534	233101031
R3	250K		20%		AB	70A4N048R254A	232002541
R4	30.1K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220230121
S1	3PDT				C&K	7301P3Y1ZB	620401201
S2	WIRING ASSY S2						A004400040
S3	WIRING ASSY S3						A004400041
S4	SWITCH,PC MTG MINI				GRAYHILL	50CP36-01-1-4N	640001200
S16	THUMBWHEEL SW,5SECT.PC MT				DIGITRAN	29-N-18	626801100
S17	SPDT	5A		28V	C+K COMP	7103P3DZB	620400300
W1	HARNESS SHEET#2						A004401012
W7	HARNESS, REAR ACCESS						A004401028
W8	REMOTE OPTION CABLE						A004401030

Table 9—3. Model 4002R Top Unit Assembly Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
MP1	CASE WELDMENT ASSY						A004401200
MP2-3	RACK MOUNT EARS DETAIL						A004401102
UNIT	O/A ASSY 4002R						A400201001
W1		6A		250	BELDEN	YELLOW 17250	932000801

Table 9—4. Model 4002R Power Supply Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
A1	96679 PWR SUPPLY A2A1						A004400025
F4-5		.3A		250V	BUSSMAN	MDL	863101500
J15	3-PIN	6A		250V	BELDEN	17252	652201700
MP1	SHIELD, PLEXIGLASS						A400200106
S15		3A		125V	SWCRFT	46206LF	645500200
T1		191A			PROFILE	2020	420100101
VR1	TO-3			-12V	NATIONAL	LM320KC-12	500003202
VR2	TO-3			12V	FAIRCHILD	7812KC	500078120
VR3	TO-3			5V	FAIRCHILD	7805KC	500078051
XF4-5	FUSEHOLDER,3AG PANEL				BUSSMAN	HKP	863000100



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